General Description

The D16G is a custom designed 16-channel programmable delay circuit. Each channel consists of an input LVDS-to-CMOS level converter; four stages of delay with 1, 2, 4, and 8 steps; and output width pulse shaper. Also, the chip has the possibility to generate a test level at each output. This option is used for testing chip-to-chip connections. The chip has a serial interface to control the delay and set the output test level.

The D16G is designed and fabricated using a CMOS 0.5 micron technology.

The chip is capsulated into a QFP-64L 10X10 plastic package.

This ASIC is designed as a part of the anode front-end electronics for Cathode Strip Chambers of the Endcap of the Muon System of CMS experiment.

Features

- Input signal level: LVDS standard
- Input resistance: 110 Ohm
- Output signal: 3.3 V CMOS
- Number of delay steps: 15
- Delay step (slope): 1-4 ns (adjustable with an external current)
- Output pulse width: 40 ns (adjustable with an external current)
- Power supply voltage: 3.3 V
- Power consumption: 0.2 W
- Temperature drift: 0.6 ns/10°C

Top View

Size: 10 mm x 10 mm x 1 mm.
Pin pitch: 0.5 mm.
16 Channel Programmable Delay

D16G

Pin Configuration

Pin 1

Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out9
Out10
Out11
Out12
Out13
Out14
Out15
Out16

Gnd
SEL
CLR B
DOUT
Iv
Vdd
Gnd
In1 P
In1 N
In2 P
In2 N
In3 P
In3 N
In4 P
In4 N

Gnd
SEL
CLR B
DOUT
Iv
Vdd
Gnd
In1 P
In1 N
In2 P
In2 N
In3 P
In3 N
In4 P
In4 N

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# 16 Channel Programmable Delay

## D16G

### Electrical Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input signal level</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LVDS standard</td>
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<tr>
<td>Input impedance</td>
<td>Rinp</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Ohm</td>
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<tr>
<td>Output signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3 V CMOS</td>
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<tr>
<td>Minimum delay</td>
<td>Tdel.min</td>
<td>Pin Id connected to Gnd via 10K, delay code 0</td>
<td>19</td>
<td>22</td>
<td>24</td>
<td>ns</td>
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<td>Delay step (slope)</td>
<td>Sd</td>
<td>Adjustable with an external current</td>
<td>1</td>
<td></td>
<td>4</td>
<td>ns/LSB</td>
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<tr>
<td>Number of delay steps</td>
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<td></td>
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</tr>
<tr>
<td>Delay nonlinearity</td>
<td></td>
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<tr>
<td>Channel-to-channel difference within chip</td>
<td>dT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Sd/2</td>
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<tr>
<td>Output pulse width</td>
<td>Tpulse</td>
<td>Pin Iw connected to Gnd via 20K.</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td>Output pulse rise time</td>
<td></td>
<td>Load capacitance 15 pF</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Output pulse fall time</td>
<td></td>
<td>Load capacitance 15 pF</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Output current</td>
<td>Iout</td>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>Vdd</td>
<td></td>
<td></td>
<td></td>
<td>3.3</td>
<td>V</td>
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<tr>
<td>Power consumption</td>
<td>P</td>
<td></td>
<td></td>
<td>0.2</td>
<td></td>
<td>W</td>
</tr>
</tbody>
</table>
16 Channel Programmable Delay

Test Performance

Delay chip distribution vs. delay at code 15.

Typical samples of delay vs. delay code. A – group 7, delay slope 2.2 ns/LSB
B – group 1, delay slope 1.5 ns/LSB
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**D16G**

**Temperature dependence**

- **Average Delay (code 0), ns**
  
  - Temperature range 36 °C - 85 °C
  - Delay drift rate - 0.6 ns / 10 °C

- **Average Delay (code 15), ns**

- **Delay slope and residual vs. temperature.**
  
  *) Maximum delay residual for code 0
  **) Maximum delay residual for code 15

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Delay Slope Tuning by Voltage

Test circuit

Delay (Va) @ code 0 = constant
Delay (Va) @ code 15 = 1.42 ns / 100 mV
Slope (Va) = 0.10 ns / 100 mV

Delay slope vs. Control Voltage.

Minimum delay (delay code 0) vs. Control Voltage.

Maximum delay (delay code 15) vs. Control Voltage.

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Delay Slope Tuning by Current

Delay (Ia) @ code 0 = constant
Delay (Ia) @ code 15 = - 1.93 ns/10 µA
Slope (Ia) = - 0.13 ns / 10 µA

Minimum delay (delay code 0) vs. Control Current.

Maximum delay (delay code 15) vs. Control Current.
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Single-Channel Structure

Time diagram:

Delay for chip:
- $T_{del} = T_0 + \Delta T_d$
- $T_0$ - minimal delay of the delay circuit
- $\Delta T_d = \Delta T_1 + \Delta T_2 + \Delta T_3 + \Delta T_4$

Delay for each stage:
- $\Delta T_i = C_i \cdot \Delta U / I_d$, $i=1,2,3,4$

Output pulse width:
- $\Delta T_{out} = C_{out} \cdot \Delta U / I_w$
- $\Delta U$ - trigger Smith threshold
- $\Delta T_i$ - delay time for each stage
- $C_i$ - delay capacitors
- $C_{out}$ - output pulse shaping capacitor
- $I_d$ - delay circuit charging current
- $I_w$ - output pulse shaping capacitor

Multiplexer logic table.

<table>
<thead>
<tr>
<th>E</th>
<th>A</th>
<th>B</th>
<th>Out</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>0</td>
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<tr>
<td>0</td>
<td>1</td>
<td>X</td>
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<tr>
<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

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Control Logic

C1, C2, ..., C16 test level bits
T1, T2, T3, T4 - delay control

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