Anode Front End Board AD16_F

User manual

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Introduction

The Anode Front End Board (AFEB) AD16_F was designed for amplifying and discriminating anode signals from the Cathode Strip Chambers (CSC). The board is optimized for the CSC of the Endcap Muon system of the CMS detector. The essential feature of the board is excellent time resolution (RMS less than 1 ns). The board is intended for use in a limited maintenance environment.

AD16_F is the production version of the AD16 board.

Construction

The AD16_F module consists of a printed board assembled with all its components. The board’s top cover has a thermo-conductive pad between the ASIC and the cover which serves two functions – it protects the board and provides heat dissipation. The input and output connectors are located on opposite sides of the board to minimize input-output cross talk.

The input connector is a SAMTEC 19X2 socket, modified to match the standard 17X2 IDC header. The top row of the input connector is a ground connection; the bottom row has input contacts.

The output connector (3M 20X3 Header) has two parts. The first one (pins 1 – 32) is the output signal contacts. The second part is an amplifier service part. This part has power supply pin 37, power control pin 35, threshold control pin 36, and test pulse pin 39. These two parts are divided with two ground pins, 33 and 34.

There are two mechanical options for the board. The first and the main option is the AFEB/p option. This option is for direct connection to the chamber. The second option is the AFEB/s option. This option is for connecting the board to the chamber with a short cable jumper. This option may be used for small chamber size (less than 1 m) and for small detector capacitance (less than 50 pf).

Circuit diagram

The AFEB AD16_F consists of the ASIC CMP16G, an ASIC input protection network and ASIC serving networks. The input protection network for each channel consists of two limiter diodes and a decoupling capacitor.

To provide stable characteristics to the boards, a power voltage regulator, TK112, is used. The regulator has a current overflow protection, overheating protection and a power on/off control feature (standby mode). Minimum 3.5 V is a “Power-ON” signal. The input power voltage range is 5.5 V - 6.0 V. The output voltage of the regulator is 5.0 V +/-0.05 V.

There are three bias voltage sources and one current source on the board to provide the normal operational regime of the ASIC.

\[ V_{gi} = 1.59 \text{ V} +/- 0.02 \text{ V} \rightarrow \text{internal reference voltage (artificial ground)}; \]

\[ V_{off} = 1.94 \text{ V} +/- 0.02 \text{ V} \rightarrow \text{additional reference voltage}; \]

\[ V_{bp} = 3.36 \text{ V} +/- 0.03 \text{ V} \rightarrow \text{PMOS bias voltage}; \]

\[ \text{Idc} = 0.1 \text{mA} \rightarrow \text{discriminator current.} \]

The discriminator threshold voltage comes from outside via the output connector. The threshold control voltage range is from 0 V to 1.5 V. The threshold control voltage is applied to all channels of the board. The board has an internal test feature. Using the input test pulse, all channels of the board fire simultaneously.

The AD16_F output signals are LVDS compatible (bipolar output current 1.5 ma).

Application note

Inasmuch as the AD16_F has one output cable with two functions (signal transmission and power supplying), it is very important to be sure that the power voltage is OFF before connect or disconnect the cable.

Troubleshooting

All boards after production are carefully tested and certified. All information is on the WEB page http://www-hep.phys.cmu.edu/cms/

In case of problems:
- Check the power voltage (5.5V – 6.0V)
- Check the “Power ON” signal (3.5 V – 5.5 V)
- Check the threshold voltage on the board
- Check the test pulse on the board (negative pulse)

If all signals are normal, try to watch the output pulse with an oscilloscope (use high impedance probe).
If there is no output pulse on the board, the board needs maintenance.
### AD16_F specification

#### General

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<th>Details</th>
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<tr>
<td>Size</td>
<td>2.8” x 3.1”</td>
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<tr>
<td>Number of channels</td>
<td>16</td>
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<tr>
<td>Input connector</td>
<td>19X2 socket SAMTEC SSQ-1-19-02-T-D-RA (modified)</td>
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<tr>
<td>Input connector specification</td>
<td>1,3,5,…,33–GND, 2–not connected, 4,6,8,…,34–INP16-INP1.</td>
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<tr>
<td>Output connector</td>
<td>20 x2 header 3M 3432-5002</td>
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<td>Installation fixture</td>
<td>Direct connection option – AFEB/p, Connection with a cable jumper – AFEB/s</td>
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#### Power characteristics

- **Power voltage**: +5.5 V - +6.0 V
- **Current**: 0.1 A
- **On board power protection**: Fully protected power regulator
- **Remote power switch**: +3.5 V – power “ON”

#### Input characteristics

- **Input impedance**: 40 Ohm equivalent
- **Input DC connection**: Capacitor decoupled
- **Spark Protection**: One stage diode protection
- **Minimum input signal**: 10 fC
- **Maximum input signal**: 1 pC
- **Maximum overflow signal**: 100 pC
- **Maximum detector capacitance**: 250 pF

#### Transfer characteristics

- **Amplifier gain**: 7 mV/fC
- **Shaping time**: 30 ns
- **Amplifier noise Cin=0**: 0.8 fC
- **Amplifier noise Cin=200 pF**: 1.8 fC
- **Threshold control**: 0 V – 1.2 V
- **Minimum threshold**: 7 fC
- **Maximum threshold**: 150 fC
- **Signal propagation time**: 67 ns
- **Slewing time**: 3 ns @ (50 fC - 500 fC)
- **Time resolution**: 0.8 ns @ 80 fC
- **Dead time**: 110 ns
- **Recovery time @ 10 pC**: 900 ns
  - @ 100 pC: 60 us
- **Maximum test pulse frequency**: 16 MHz

**Output pulse:**

- **Signal levels**: LVDS compatible 1.5 mA
- **Output driver capability**: 110 Ohm load
- **Output pulse width**: Input pulse width over the threshold
- **Leading edge**: 6 ns
- **Trailing edge**: 6 ns
Test Pulse parameters
Test pulse is a positive levels pulse
Amplifier is triggered by the negative transition of the test pulse.

- Minimum level: 0 V
- Maximum level: +5V
- Termination: 110 Ohm
- Minimum pulse amplitude: 10 mV
- Maximum pulse amplitude: 500 mV
- Leading edge: 20 ns
- Trailing edge: 20 ns
- Negative pulse width minimum: 500 ns
- *Internal injection capacitance: ~0.25 pF

Notes:
*) Parameters are tested for each board. Results are on the WEB page:
**) Dead time definition: Threshold – 20 fC; First pulse amplitude – 110 fC; Second pulse amplitude – 40 fC
The dead time is defined as a minimum time interval between pulses when the second pulse has a 50% of registration efficiency.
***) Recovery time defined for the second pulse amplitude – 40 fC
****) Crosstalk level is defined as an equivalent input charge induced by an adjacent input circuit plus the fired discriminator reflection.
Top view.

- Input Power Voltage contact.
- Power regulator
- "On board" power voltage contact.
- Input connector.

Bottom view

- Power "ON" signal
- Input Power Voltage.
- ASIC test channel output.
- ASIC test channel input.
- Threshold control voltage contact.
- Test Pulse contact.