

Summary for the Test Stand Status

	System	Capability	Ubility	Equipment	Preparedness
Quick Board Test Stand	Windows 95	Board Quality Quick Test	ACC	Full Set	Ready, Sent to ACC
Quick Chip Test Stand	Windows 95	Chip Quality Quick Test	Fermilab	Full Set	Ready
Final Test Stand	Linux	Full Test		Main Set	Under construct

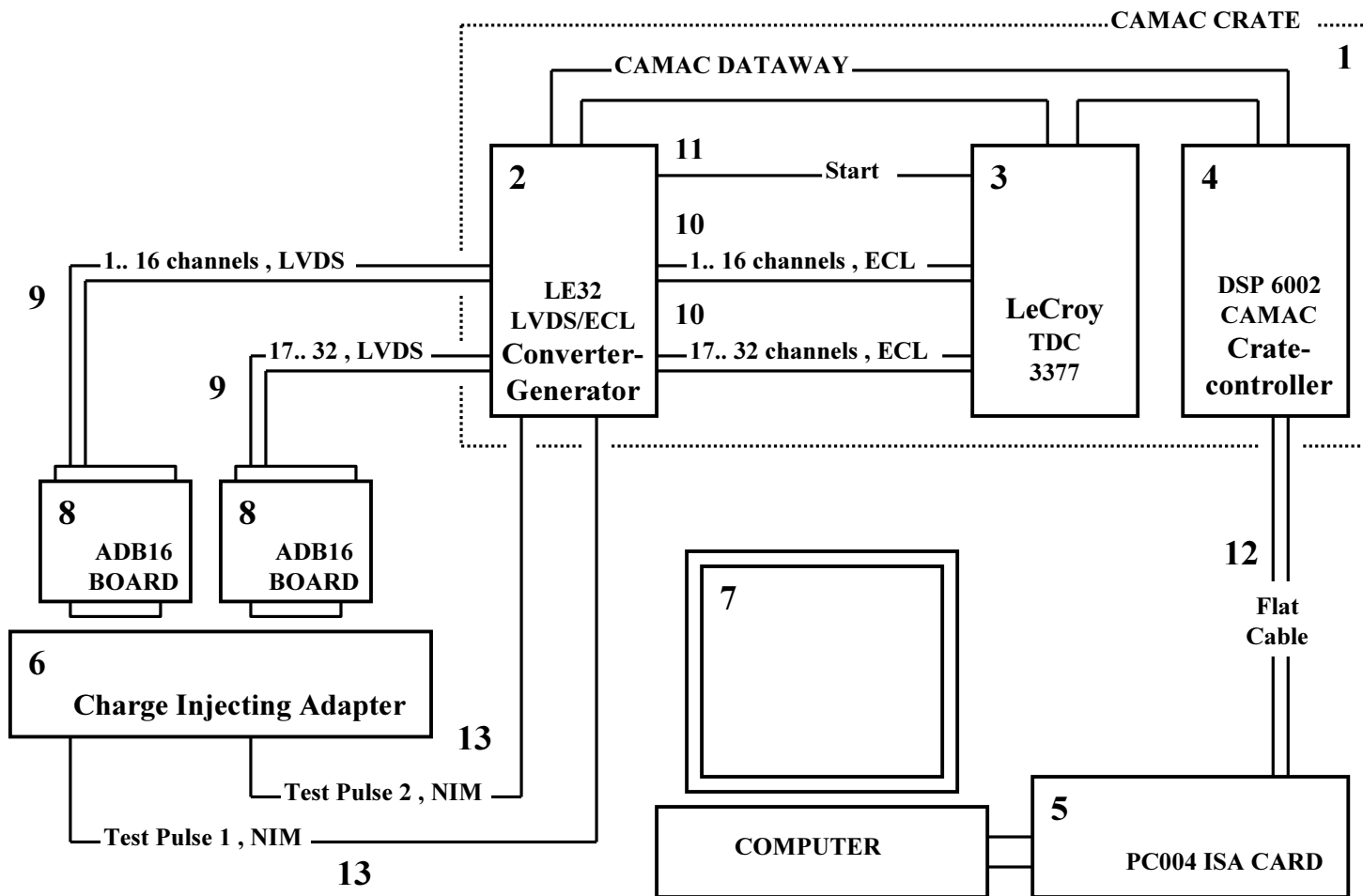
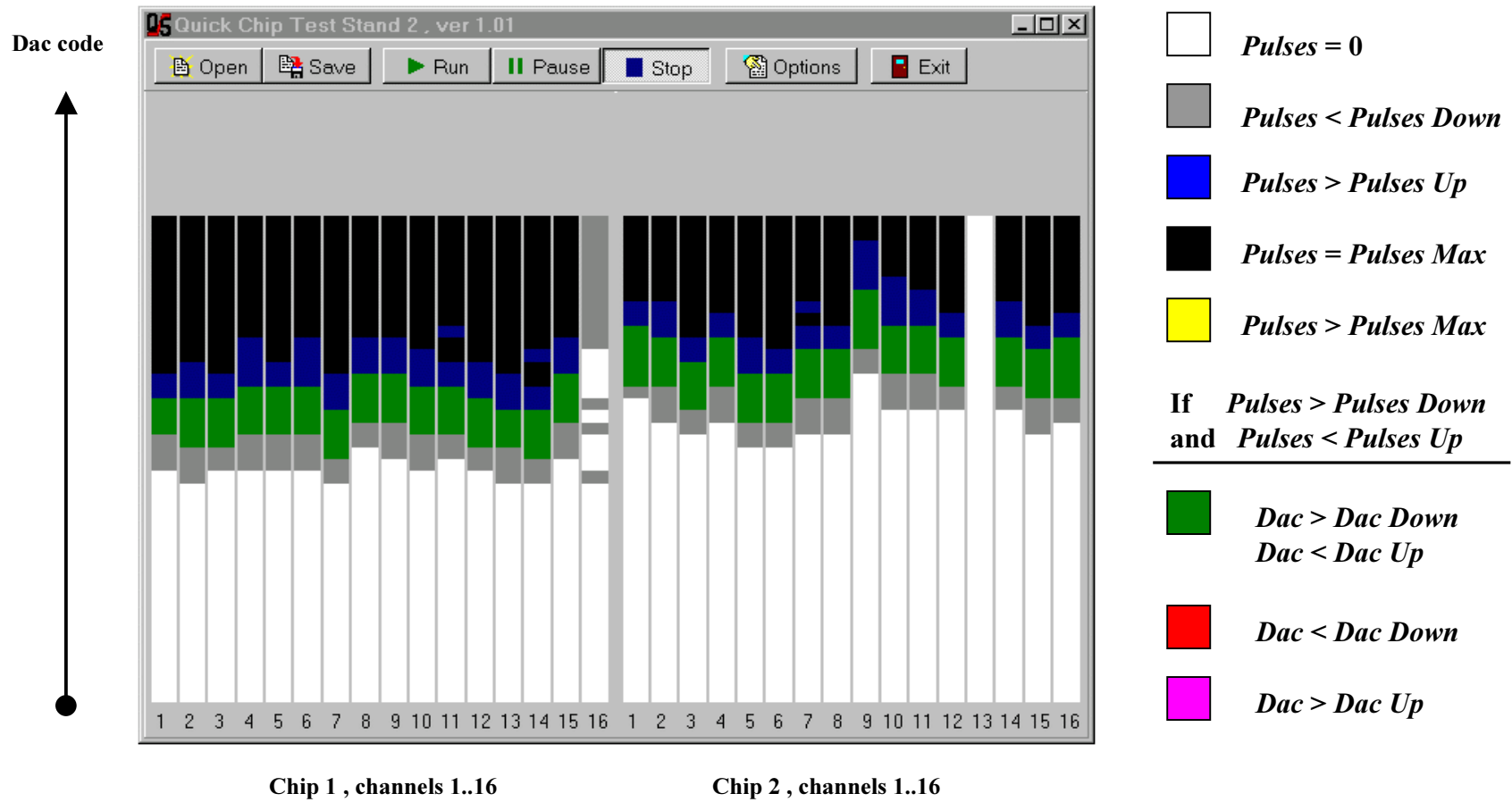
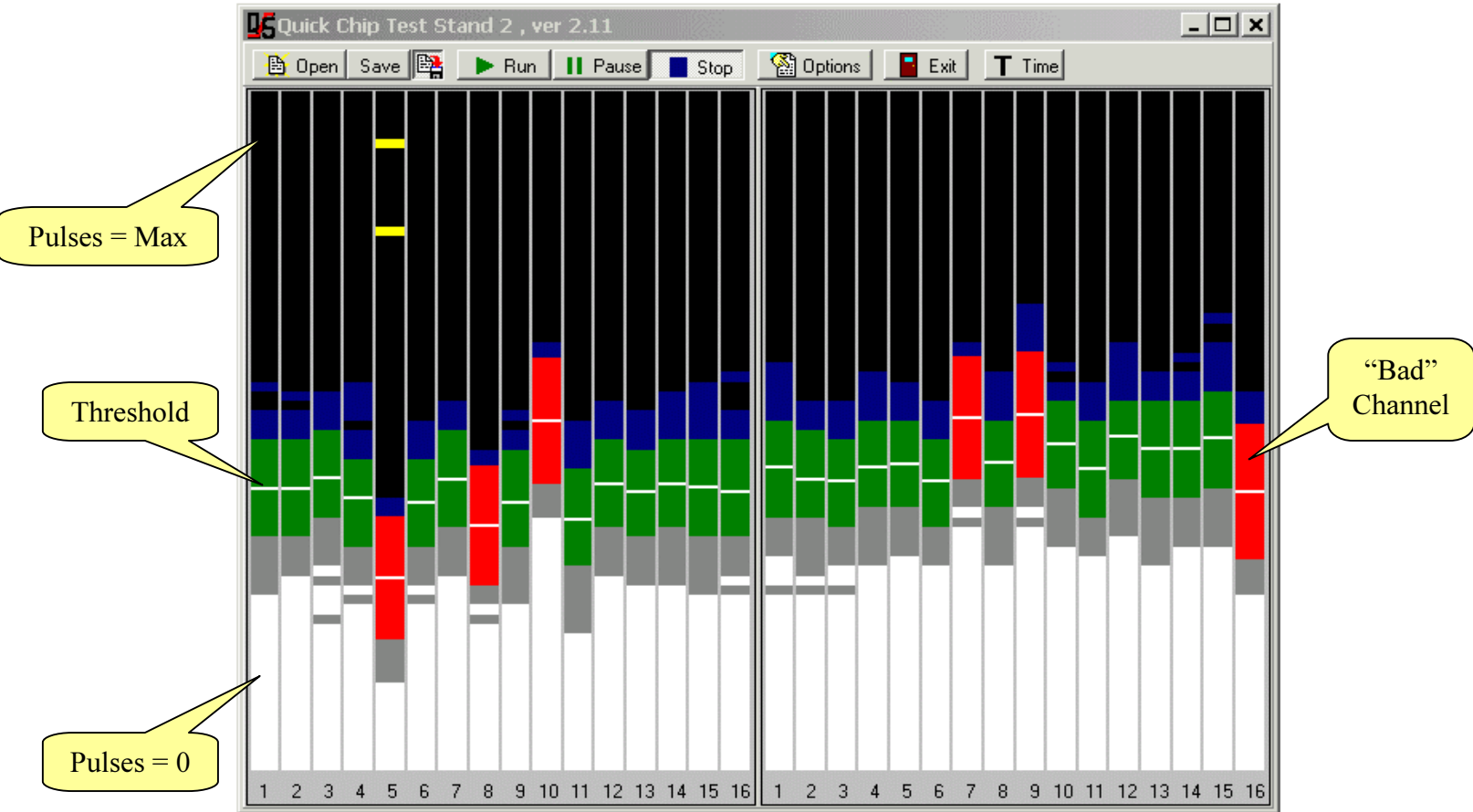


Fig.1 Quick Chip Test Stand , Hardware Scheme.

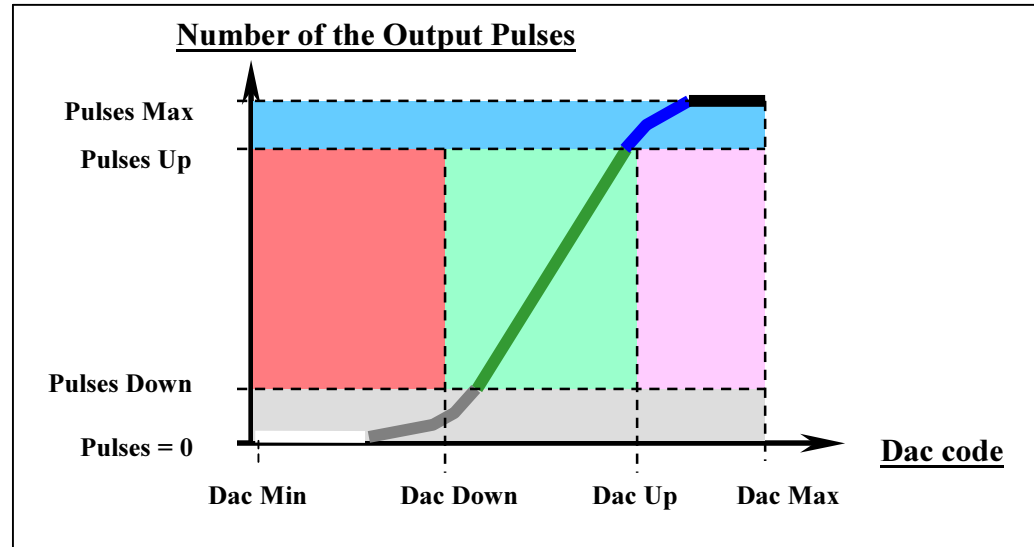
Fig.2 Quick Board Test Stand



Visual Control for Two Chips



Threshold Efficiency (Number of the pulses vs Dac code)



Color of the curve in the Threshold efficiency.

-
1. *Pulses equal 0*
 2. *Pulses not equal 0 and Pulses less then Pulses Down.*
 3. *Pulses equal Pulses Max*
 4. *Pulses not equal Pulses Max and Pulses less then Pulses Down.*
 5. *Pulses greater then Pulses Down and Pulses less then Pulses Up*
 - a) *Dac less then Dac Down*
 - b) *Dac greater then Dac Up)*
 - c) *Dac between Dac Up and Dac Down*
 6. *Pulses greater then Pulses Max*

White

Gray

Black

Blue

Red

Purple

Green

Yellow

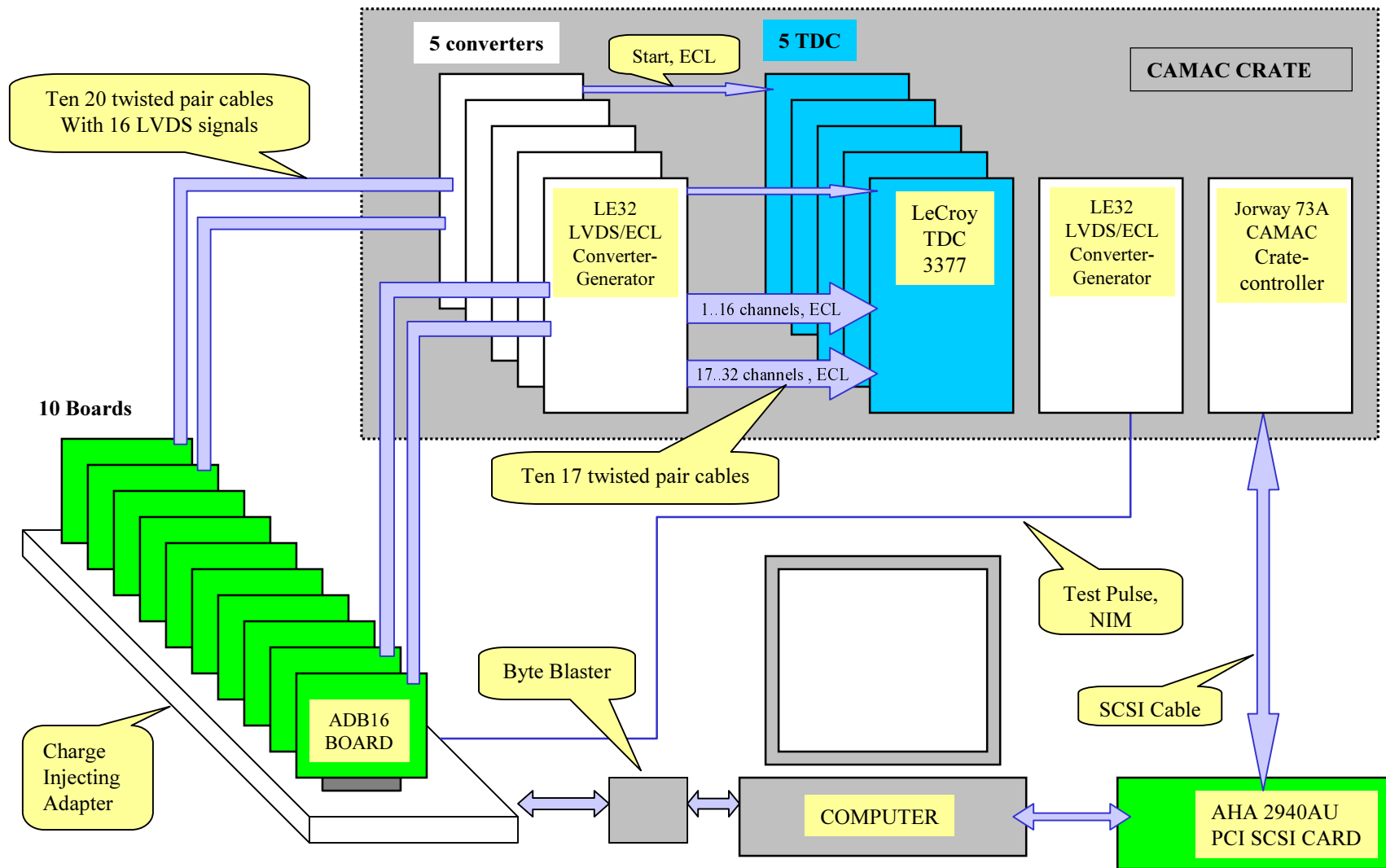


Fig.3 ADB16 Board Test Stand , Hardware Scheme.

Efficiency Measurements

Raw table for each chip
Pulse Number vs DAC code

Calculating Parameters for the Each Channel

Threshold

RMS Noise

Threshold Error

Noise Error

“Bad” channel selection

Summary Parameters for the chip

1. Minimal Threshold
2. Maximal Threshold
3. Maximal Threshold Error
4. Maximal Noise
5. Maximal Noise Error

Visual Control for “bad” Efficiency

Exceeding Parameters

Check for Good Efficiency

1. Threshold Region
2. Max Threshold
3. Max Noise

Delay Measurements

Raw table for each chip
Delay vs DAC code

Calculating Parameters for the Each Channel

Minimal Delay

Maximal Delay

Slewing Time

All parameters are calculated
in the defined DAC region

“Bad” channel selection

Summary Parameters for the chip

1. Minimal Delay
2. Maximal Delay
3. Slewing Time for Whole Chip
4. Maximal Channel Slewing Time

Visual Control for “bad” Delay

Exceeding Parameters

Check for Good Delay Characteristic

1. Delay Region
2. Max Channel Slewing Time
3. Max Chip Slewing Time