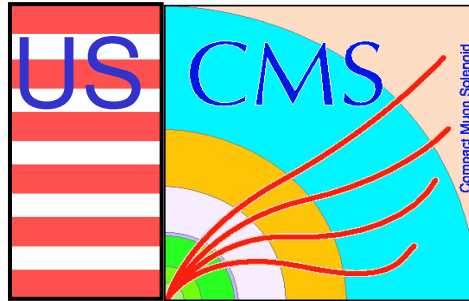


Test Beam Results Of Front End Timing



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Outline

- **Sep-Oct '04 beam test conditions**
- **CSC front-end timing**
- **Anode front-end timing**
- **Cathode comparators timing**



Sep-Oct '04 beam test conditions

- **Beam**
 - Asynchronous (1.5 week)
 - 25 ns structured beam (1 week)
- **Setup features**
 - 5 CSCs, 3 RPCs, HCAL
 - 4 peripheral crates
 - New DDU/DCC
 - TrackFinder crate (SP1+SP2)
 - Trigger: SC (Scint. Counters), TF (Track Finder)
- **Details and main results in EMU Oct 2004 talks by**
 - F.Geurts, D.Acosta, A.Korytov, M.Von der Mey, J.Hauser, S.Durkin





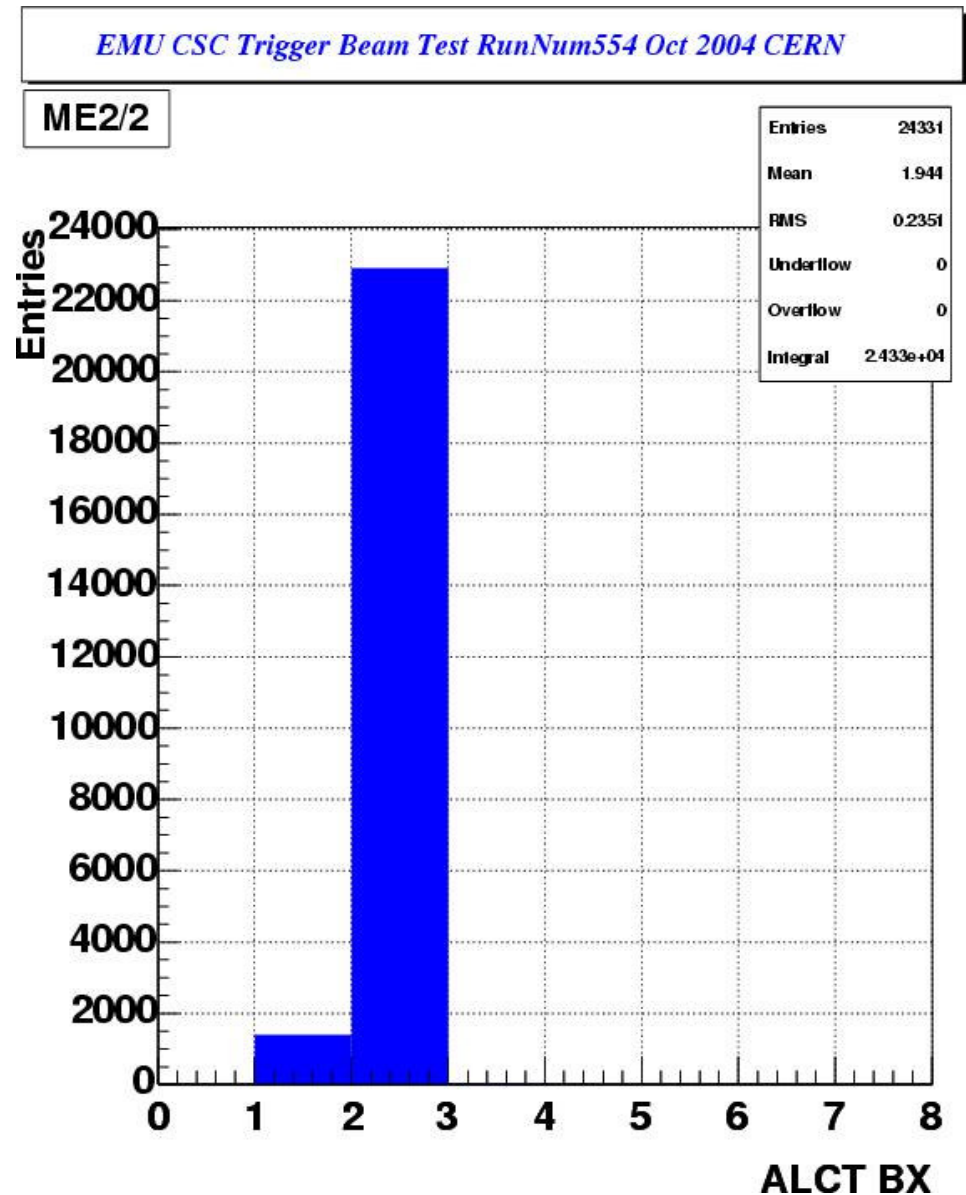
CSC front-end timing

- **CSC synchronization – complicated and challenging procedure**
 - See details, plan and extensive discussion in the EMU Oct 2004 talk by J. Hauser
- **AFEB timing in the 25 ns beam tests**
 - Scan 0-25 ns ALCT delays in 2.2 ns steps to get >99% ALCTs BX occupancy in one BX 25 ns time bin
 - Set one and the same best delay for ALL AFEBs of given CSC (no individual settings)
 - No AFEB nominal 20 fC threshold settings (ALCT DACthr = 20 setting gives Qthr = 20 - 35 fC)
- **AFEB individual delay and threshold settings will be done in future CSC synchronization**



Anode front-end timing

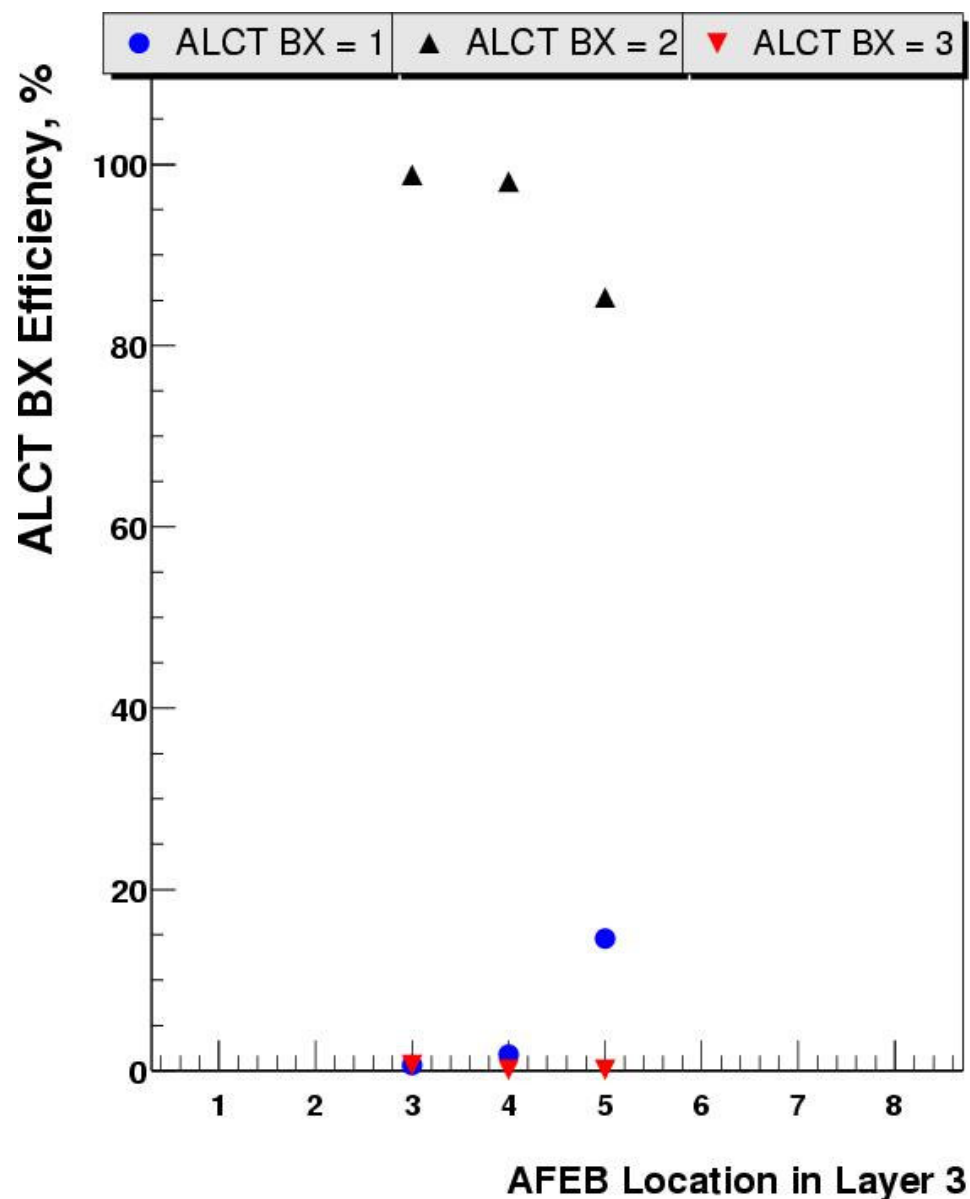
- In most cases in the 25 ns beam test the ALCT BX one 25 ns bin efficiency was $> 99\%$ with no individual fine delay tuning done
 - Hits are in a compact group of a few AFEs for SC trigger (similar cable lengths)
 - Delay chips in each given ALCT board have similar delay characteristics
 - ALCT delay was set so that ALCT BX = 2 was the most likely
- In cases of the ALCT BX efficiency of $\sim 95\%$ (see Fig.)
 - More peripheral AFEs involved in TF trigger
 - The ALCT BX one bin inefficiency is tracked down to AFEB/ALCT delay chips which need the fine delay tuning





Anode front-end timing (cont'd)

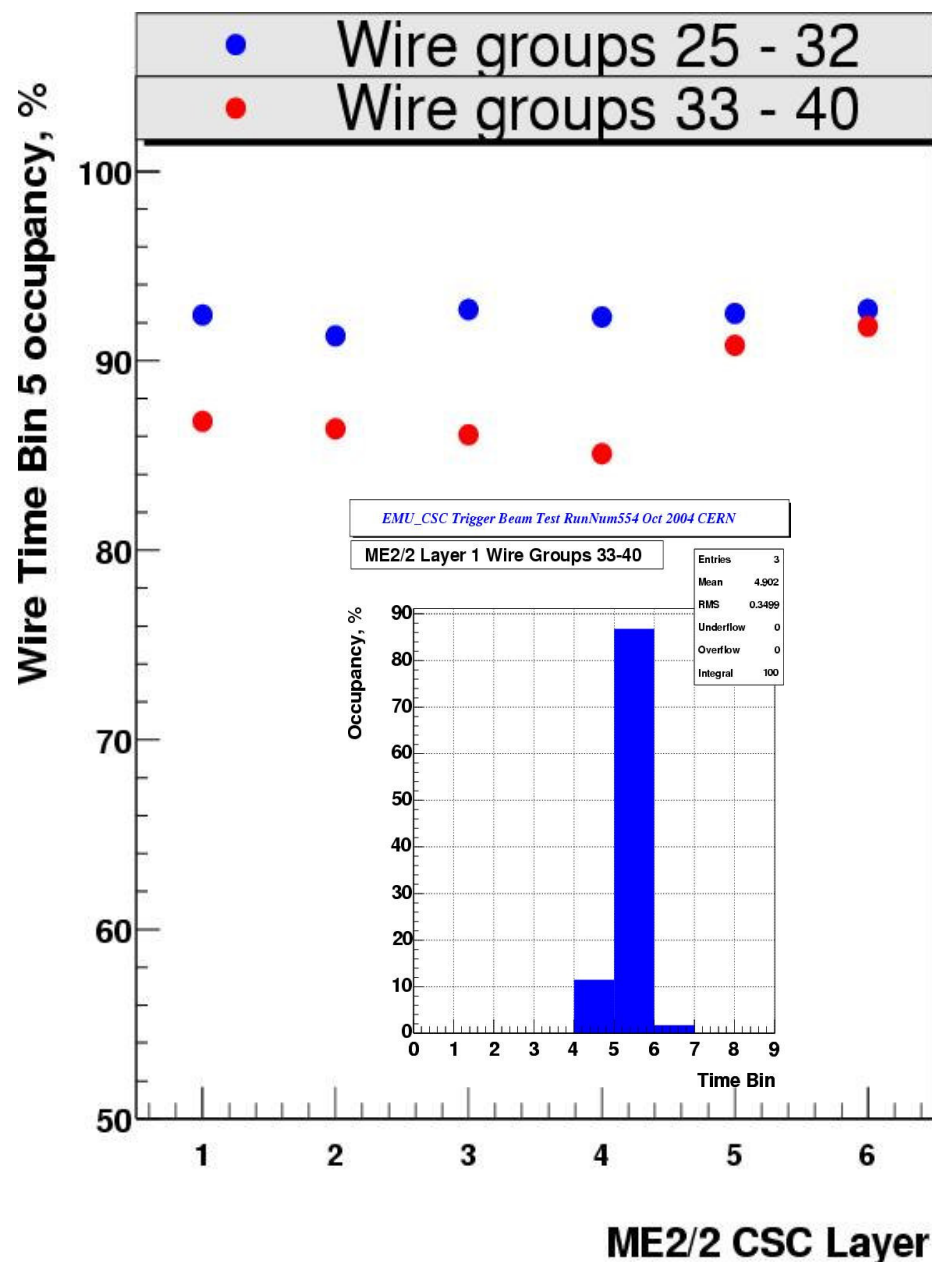
- **ALCT BX efficiency vs AFEB location**
 - Choose events with one anode wire group hit and one cathode comparator hit in each layer of ME2/2 (Run 554, TF trigger)
 - Look at single ALCT track events
 - ALCT BX one bin efficiencies vs ALCT track location in layer 3, see Fig.
(one AFEB serves 8+8 wire groups in 2 CSC layers, therefore 8 AFEB locations in one layer with 64 wire groups)
 - ALCT delays for AFEBs in location 5 need tuning





Anode front-end timing (cont'd)

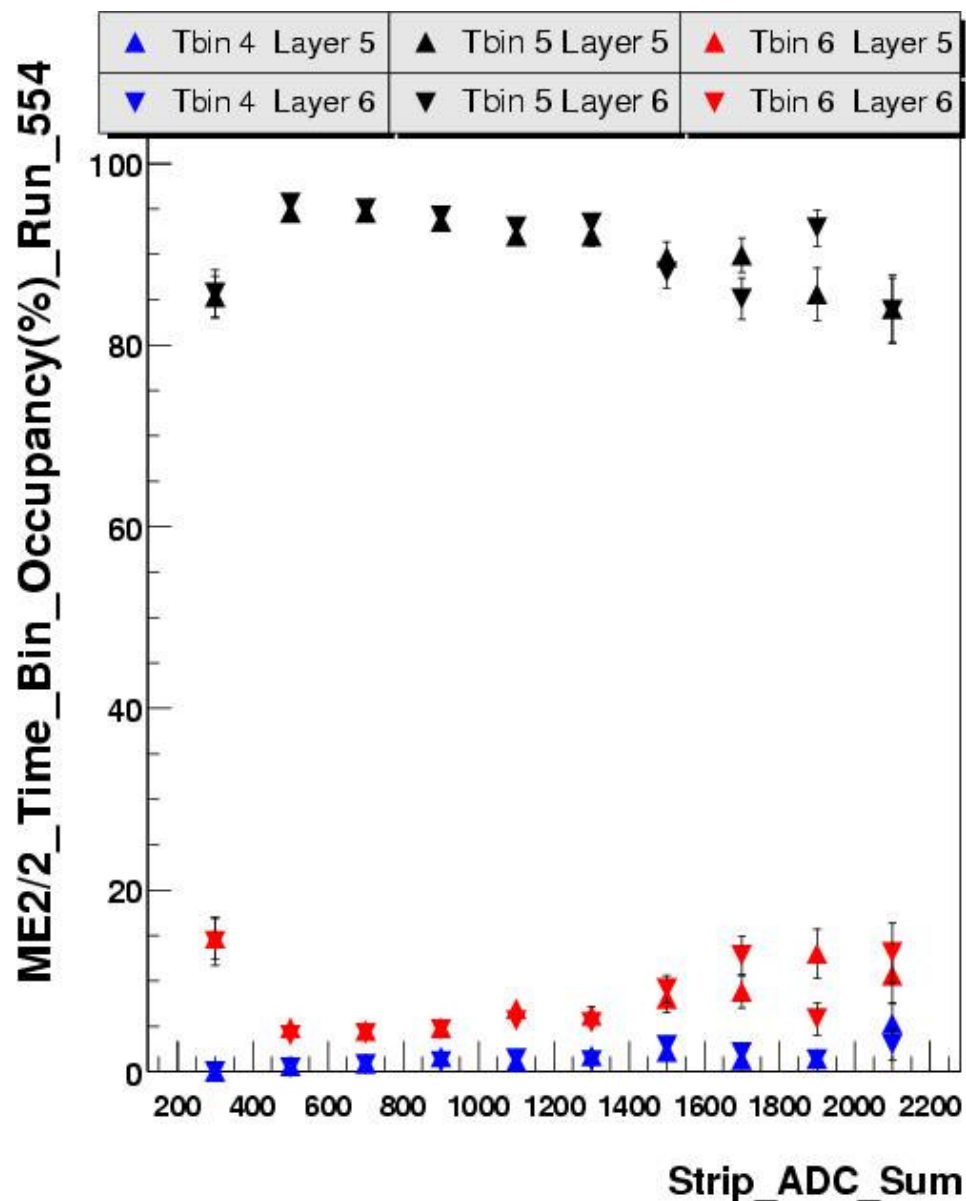
- **AFEB one time bin occupancy**
 - Look at max. occupancy in time bin 5 (Bunch Crossing Number BXN=5)
 - ALCT delays for AFEBs with wires 33–40 in layers 1 – 4 need fine tuning
- **For ALCT delay tuning**
 - Find optimum delay for each AFEB using results of the ALCT delay scan
 - Rescan ALCT delay with fewer 2.2 ns steps around delays with max. AFEB's one time bin occupancy to confirm higher ALCT BX efficiency





Anode front-end timing (cont'd)

- **AFEB time bin occupancy vs cathode signal amplitude (see Fig.)**
 - Single anode wire hit and single comparator hit per plane
 - Look at normalized occupancies (time bins 4 - 6) vs cathode signal amplitude
 - In general agrees with slewing time data from the AFEB test stand



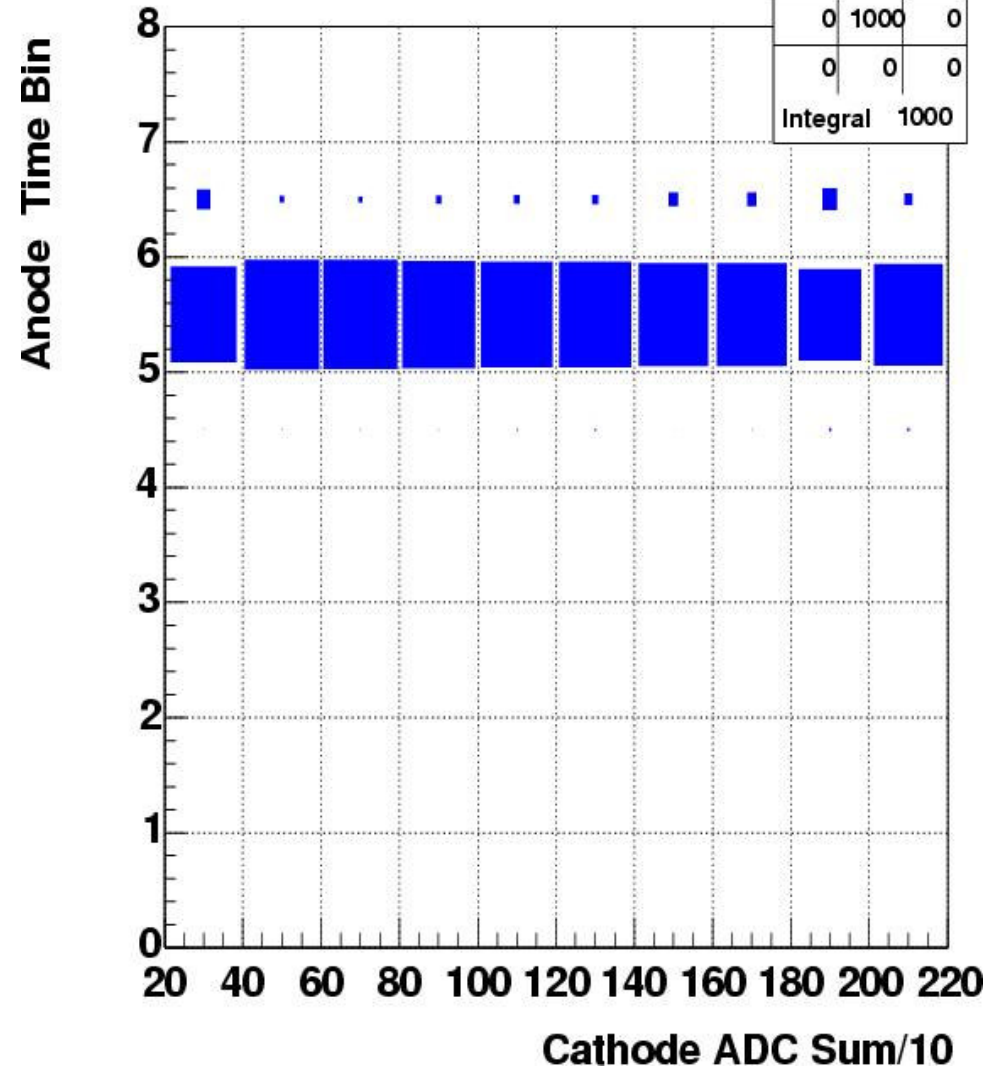


Anode front-end timing (cont'd)

EMU CSC Trigger Beam Test RunNum554 Oct 2004_CERN

ME2/2 Layer 2

Entries	30	
0	0	0
0	1000	0
0	0	0
Integral	1000	

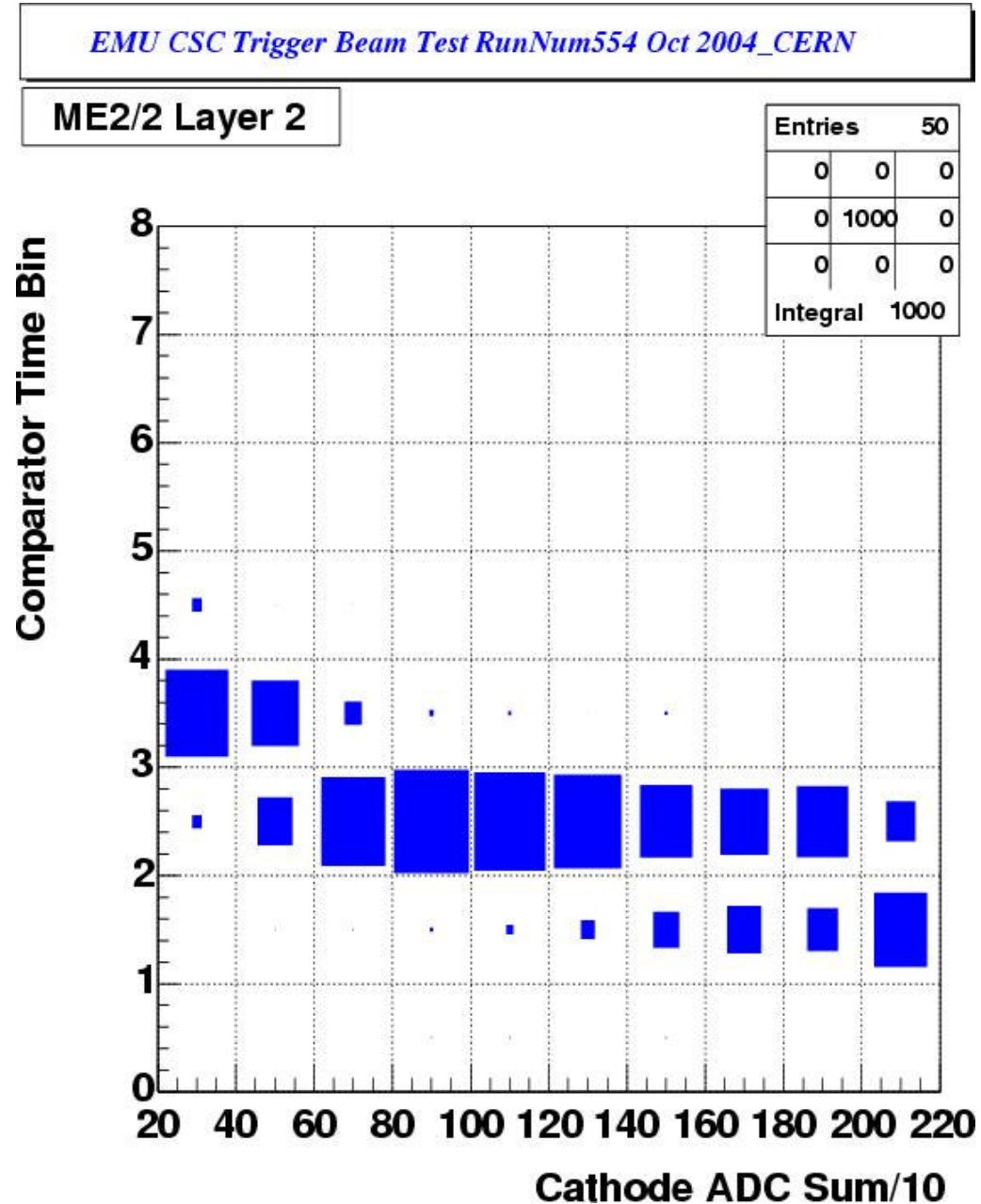


- 2D presentation of the anode time vs total cathode charge



Cathode comparators timing

- **Cathode comparator time vs total cathode signal charge (see Fig.)**
 - Single anode hit and single comparator hit (Strip #42)
 - Occupancy is normalized at each amplitude bin
 - Comparator time is within three 25 ns time bins





Conclusion

- **The beam test data confirm that:**
 - ALCT individual delay settings for AFEBs will improve ALCT BX efficiency (as expected)
 - The AFEB one time bin occupancy to be used in the delay tuning.
- **Future plans – continue analysis and compare the beam test data with ORCA simulation/digitization:**
 - Cathode signal amplitude vs time bin
 - ORCA Muon tracking in the beam test data for all four CSC?