Anode front-end electronics.  
Current status

• AFEB production schedule  
  - CMP16-G chip first test results  
  - AFEB production schedule  
  - AFEB test procedure  
  - AFEB certification  
• AFEB-ALCT cable production schedule  
• AFEB input cable production  
• Delay chip DEL16 “first look” test  
• Delay chip test procedure
US CMS EMU meeting

Amplifier ASIC CMP16_G status

1. Pre-production shipment
   - Produced          1900 chips
   - Selected “good” chips  1150 chips
   - Yield rate       60%
   -

2. Production shipment (September 22)
   - Produced quantity  25000
   - Expected yield rate 60%
   - Expected good chip quantity 14000
   - Tested           2500
   - Good chips       1650
   - High threshold chip 600
   - Low threshold chip  40
   - Bad chip         200
### AFEB Production Schedule

**Total AFEBs:** 10544  
**Flat plank option:** 9212  
**Tray option:** 1332

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**Note:** The table details the production schedule for AFEBs, including chip production, incoming inspection, and various other stages of the production process. The totals are provided for each stage across different calendar years (2001 to 2004).
AFEB production rate

Production rate

Delivery rate

CY2001  CY2002  CY2003
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Anode electronics test

Test stand adapted for 10 amplifier boards

Test stand structure:
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Test 1- good chip selection.

Test condition:

Power voltage -5.5V
Threshold voltage -150 mV (~20 fC of input charge),
Amplifier input capacitor - 0 pF
Input charge scan range - 0 fC -200 fC.
Input signals come through internal capacitance

Clamp-shell adapter for two chips.

Good chip requirements:

-noise level - less than 0.8 fC @ Cin=0 pF;
-threshold uniformity better than +/- 10%;
-propagation time variation - within 4ns for all channels of the chip for input signals from 50 fC to 200 fC.
Test 2 - Burn-in procedure

Burn-in procedure.

- Oven temperature  - 100° C
- CMP16 power on  - 5.5V
- Threshold voltage  - 150 mV
- Input test pulse amplitude  - 150 mV.

Burn-in test duration  - 75 hours.
Test 3 - board certification

10 boards test adapter

- amplifier input capacitance
  \(C_{in} = 200\text{pF}\)
- individual injection circuit for each channel with accuracy better than 2%

4 test runs:
1. low threshold, external injection circuit;
2. high threshold, external injection circuit;
3. low threshold, the chip internal capacitance as an injection circuit;
4. low threshold, time measurement.
The following parameters are measured:
1 - Threshold level as a function of threshold voltage
2 - Threshold uniformity for each chip
3 - Noise level at Cin=200 pF
4 - Propagation time as a function of the input signal amplitude
5 - Propagation time uniformity
6 - Time resolution of the chip
7 - Test pulse injection capacitance of the chip calibration
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AFEB-ALCT cable production

Scheduled cable production

Acumulated cables

ME234/2
ME2/1
ME3/1
ME4/1
ME1/2
ME1/3


CY2001 CY2002

N.Bondar, October 5, 2001
Input cable specification:
Inp1 - 2.5” - 1332 cables.
Inp2 - 5.0” - 1332 cables.
Inp3 - 7.5” - 1332 cables.

Material:
.050” Pleated Foil Shielded Cable
3M 90404 Series
Flat, Halogen Free

Production:
SUB-SEM, Inc.
Expected delivery time - December 2001
Delay chip DEL16.

Produced 25000
Tested 1600
Rejected 30
Yield rate \( \sim 98\% \)

Problem:
Relatively large delay variation at maximum delay code
Relatively large delay step variation

We need to modify the test program for “on-line” delay chip selection.

Expected yield rate after selection 60\%
Delay chip mass production test

Clamp-shell adapter for two DEL16 chips

The delay chip test procedure:
1. Delay measurements
   - scan delay code in the DEL16 chip in steps of “one”
   - 100 input pulses are sent to the chip inputs for each delay step
   - the propagation time for each step is measured with the TDC modules.
2. The Output Test Level measurements
A good chip should satisfy the following conditions:
- the maximum delay and output pulse width should meet the specifications,
- the delay step variation between channels must be less than half of the delay step,
- the control interface can switch on the Output Test Level at the chip outputs.