



16 Channel Amplifier-Discriminator ASIC

CMP16_G

General Description

The CMP16_G is a custom designed 16 channel Amplifier-Discriminator for anode signal of proportional chambers. The circuit optimized for detector capacitance up to 200 pF and detector size up to 1.5 x 3.4 m². The ASIC combines low power consumption (30 mW/channel) with excellent time resolution (~2 ns). The CMP16_G is designed and fabricated using a BiCMOS 1.5 micron technology. The chip is capsulated into a QFP-80L 14X20 plastic package. This ASIC is designed as a part of the anode front-end electronics for Cathode Strip Chambers of the EndcapMuon System of CMS experiment.

Features

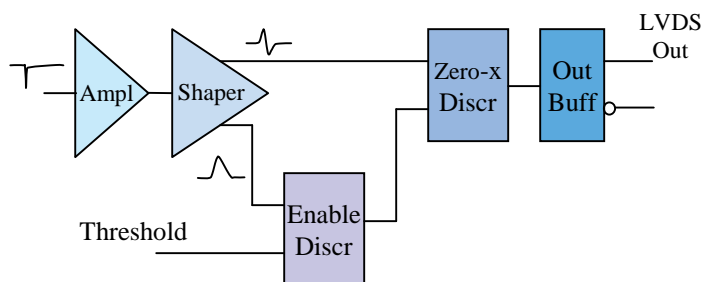
Input impedance	40 Ohm
Shaper peaking time	30 ns
Shaped waveform Semi-gaussian with Two-exponent tail cancellation	
Two level constant fraction discriminator	
Discriminator slewing time	3 ns
Low power output buffer	
Output signal LVDS compatible	1.5 mA
Power supply voltage	5 V
Power consumption	0.5 W/chip
Output signal	LVDS standard

Top View



Size: 14 mm x 20 mm x 2 mm
Pin pitch: 0.8 mm.

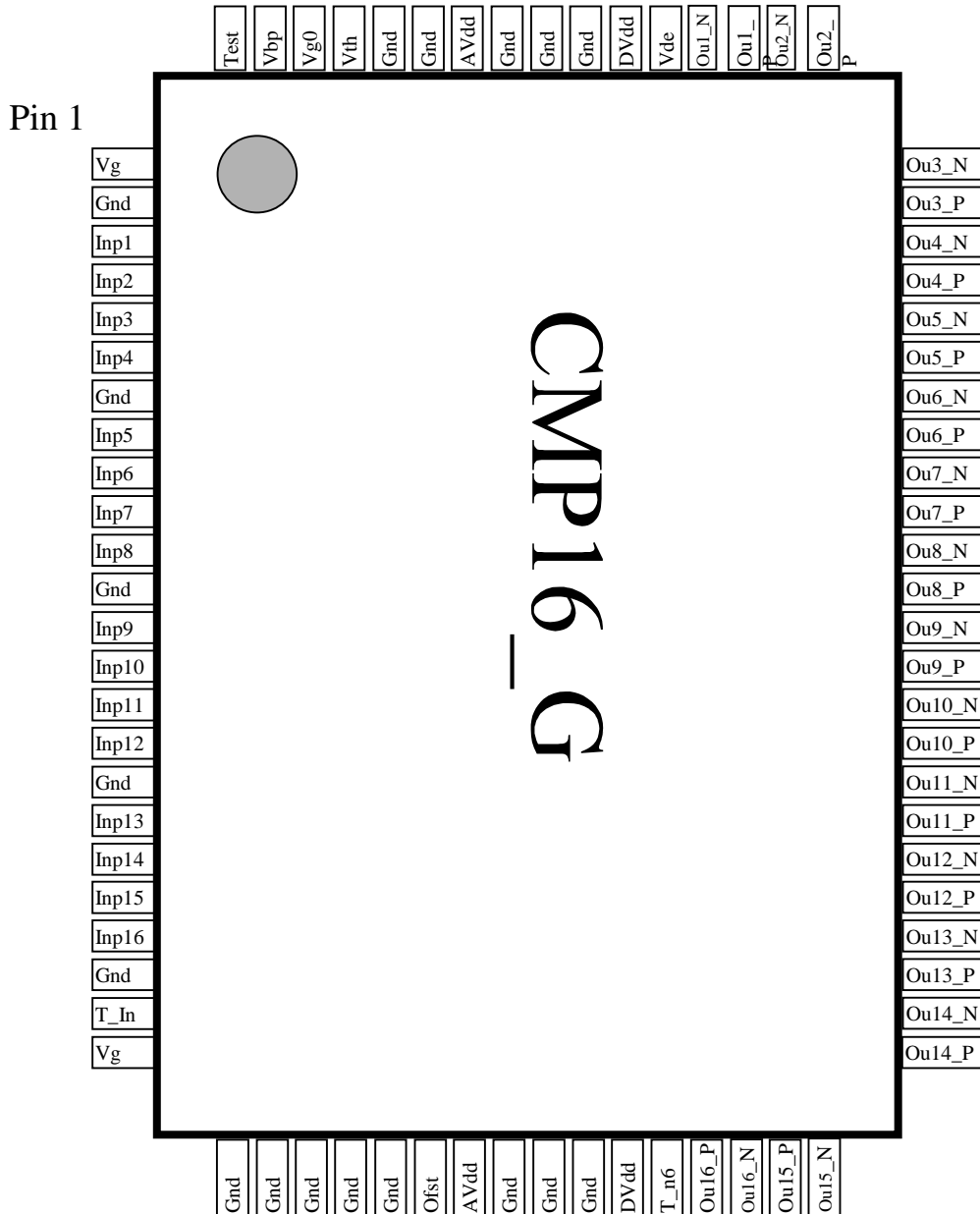
Block Diagram



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Pin Configuration



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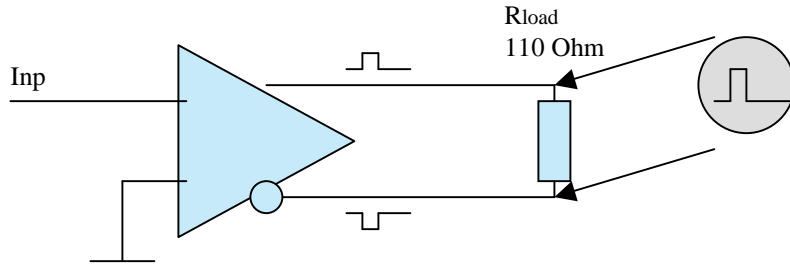
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Electrical Characteristics

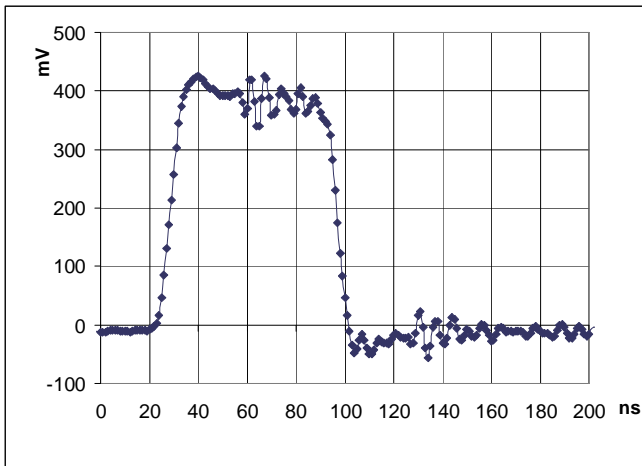
PARAMETER	SYMBOL	CONDITIONS COMMENTS	MIN	TYP	MAX	UNIT
Input impedance	Rin			40		Ohm
Peaking time	Tsh	Shaped waveform - semi-gaussian with two-exponent tail cancellation.		30		ns
Equivalent input noise	Qn	C input = 0 pF C input =180 pF	1.3	0.7 1.4	1.6	fC
Input charge range	Qin	Amplifier works without saturation.	-10		1,000	fC
Maximum allowed charge	Qmax	An external protection circuit is required for input charge higher than that limit.			100,000	fC
Threshold range		Adjustable with external voltage setting.			100	fC
Threshold voltage setting range	Vth	Linearly controlled range.	-0.1		1.0	V
Relative gain (Threshold control slope)	G	The relative gain is defined as a following ratio: $G = (V_{th1} - V_{th2}) / (Q_{in1} - Q_{in2})$	6	6.9	7.7	mV/fC
Threshold voltage offset	Vth.off	Opposite number of an external voltage value for setting threshold to zero.	0	50	110	mV
Threshold temperature dependence				+/- 0.02		fC/ °C
Discriminator slewing time	Tsl				3	ns
Propagation time	Tp		64	67	72	ns
Propagation time temperature dependence	ΔT_p			0.27		ns/ °C
Dead time	Tdt	Threshold is set to 20 fC. First pulse amplitude - 110 fC . Second pulse amplitude - 40 fC. The dead time is defined as a minimum time interval between pulses when the second pulse has a 50% of registration efficiency.		110		ns
Recovery time	Tr	Input charge 10.000 fC		900		ns
Crosstalk		Crosstalk here is defined as an equivalent input charge induced by an adjacent input circuit plus the fired discriminator reflection, determined as a percent of input charge.		0.25		%
Internal test capacitance	Ct		0.2	0.24	0.3	pF
Output pulse width	Tout	Equal to the input pulse over the threshold. Input pulse is a delta pulse with an amplitude range 2 – 20 of threshold level.	50	80	110	ns
Output signal LVDS compatible	Iout			1.7		mA
Power supply voltage	Vdd			5		V
Power consumption	P			0.5		W

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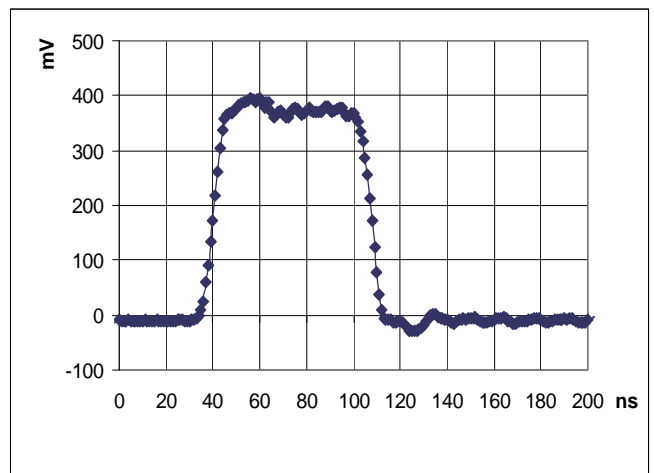
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Output pulse measurement scheme



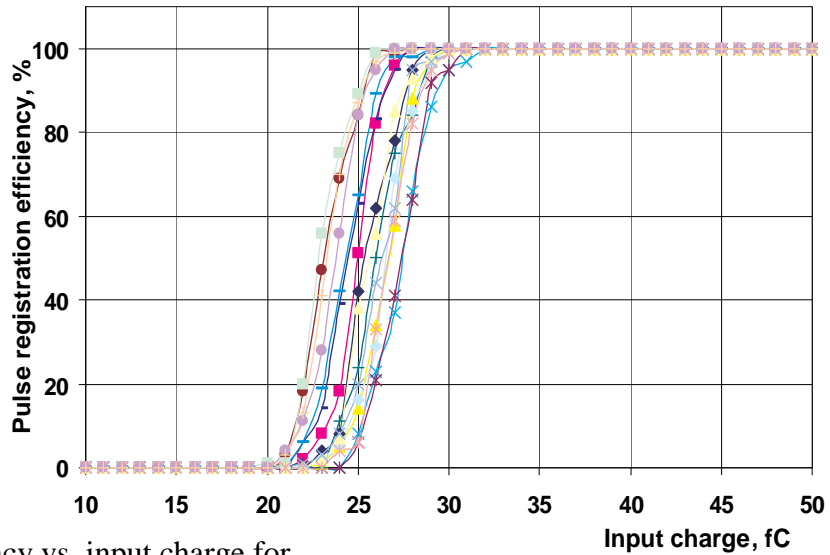
Differential output pulse waveform.
Typical sample.



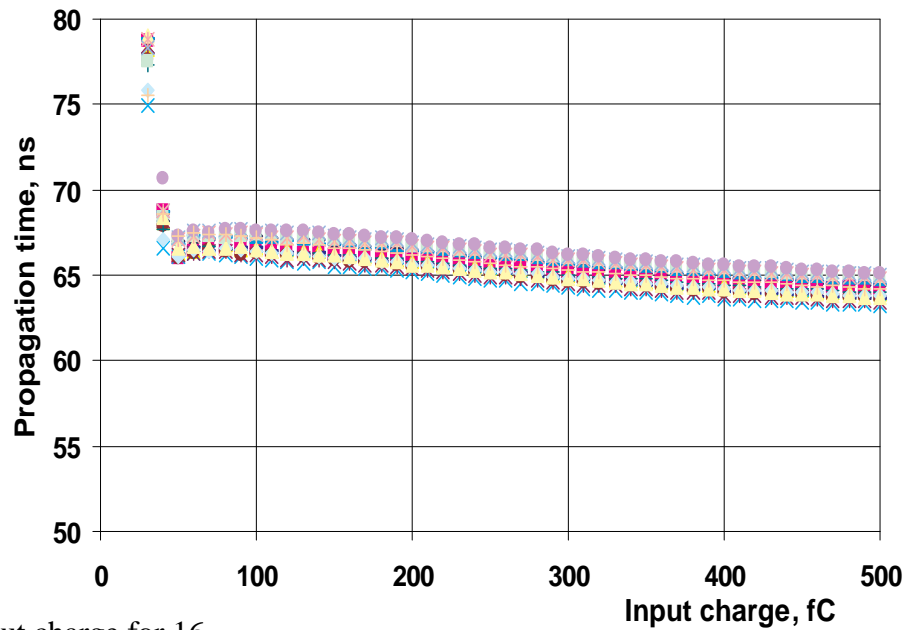
Output pulse waveform.
Averaged pulse.

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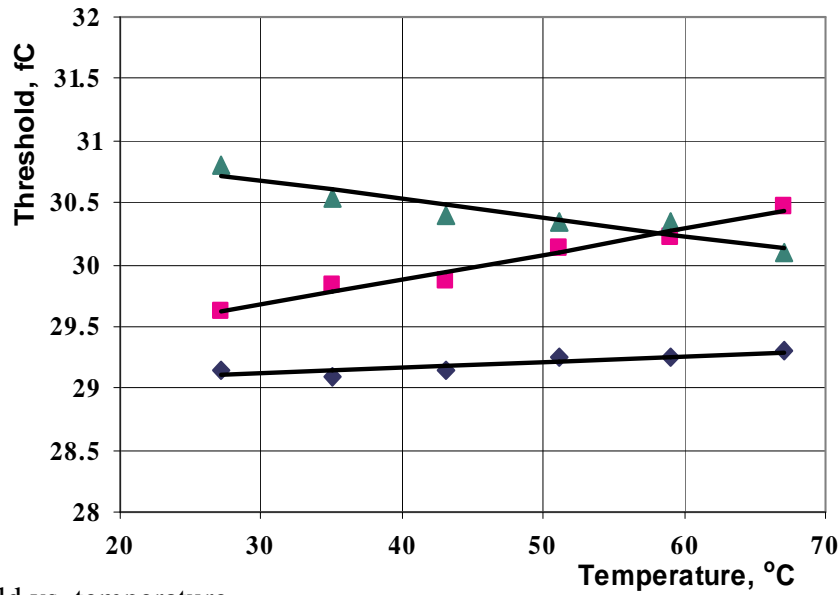


Discriminator efficiency vs. input charge for 16 channels of one chip.
Threshold set to 25 fC. Typical sample.

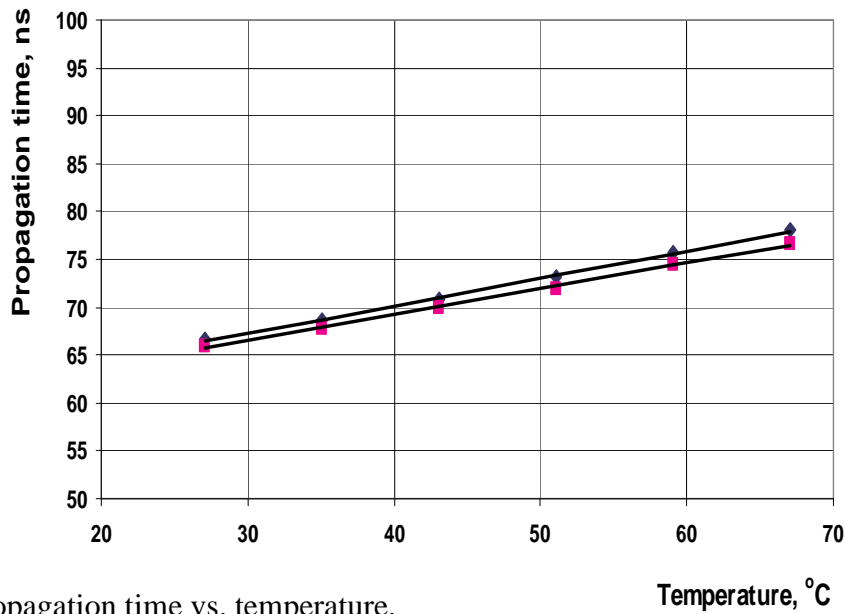


Propagation time vs. input charge for 16 channels of one chip.
Typical sample.

Temperature dependence



Threshold vs. temperature.
Three typical samples.



Propagation time vs. temperature.
Two typical samples.

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Single-Channel Schematic Diagram

Input – Input signal terminal
OutN – Output Negative signal
OutP – Output Positive signal
Threshold – Relative threshold voltage
I_{discr} – Discriminator current
V_g – Reference voltage “Artificial Ground”
Ofst – Bipolar pulse shaper reference voltage

