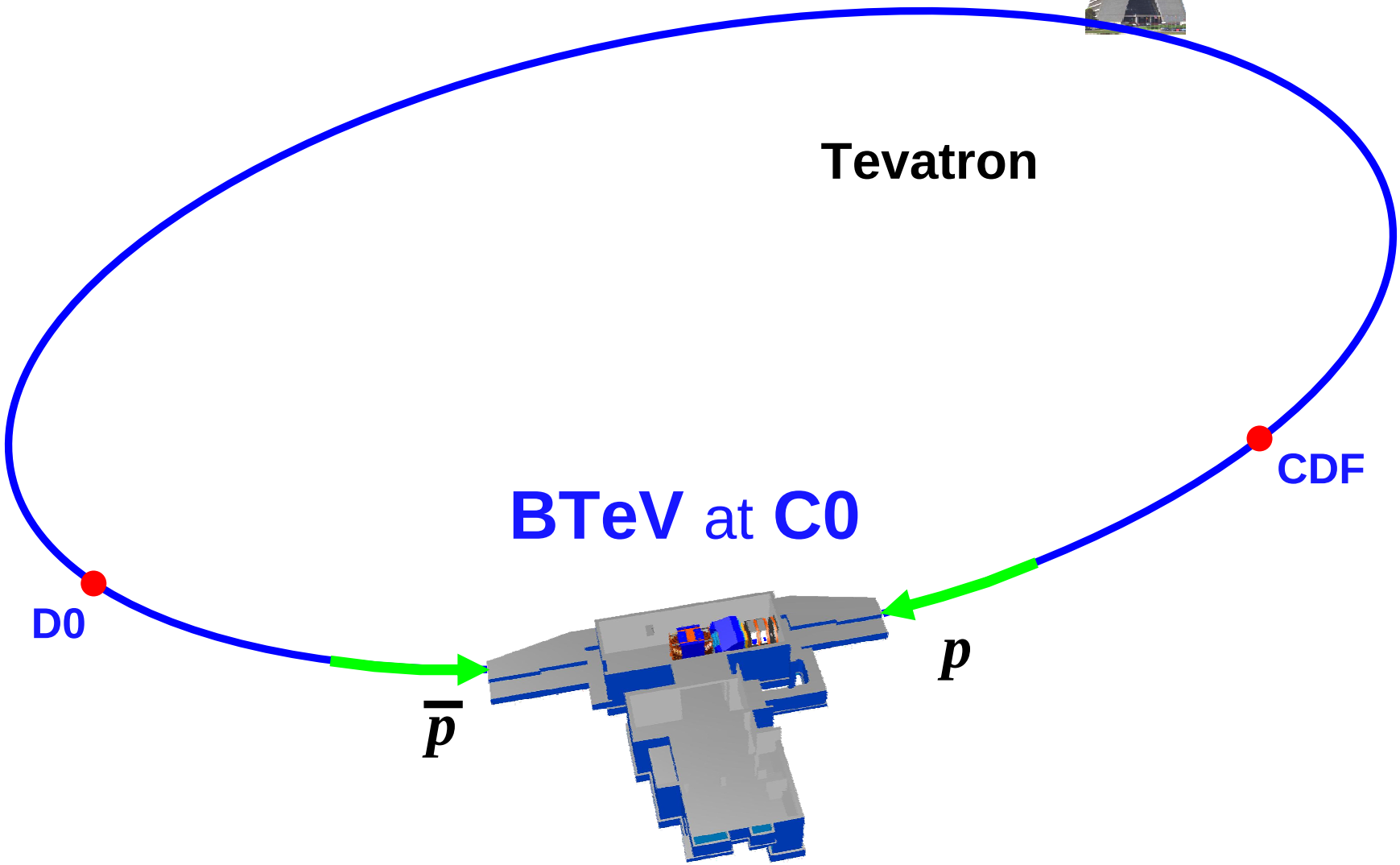
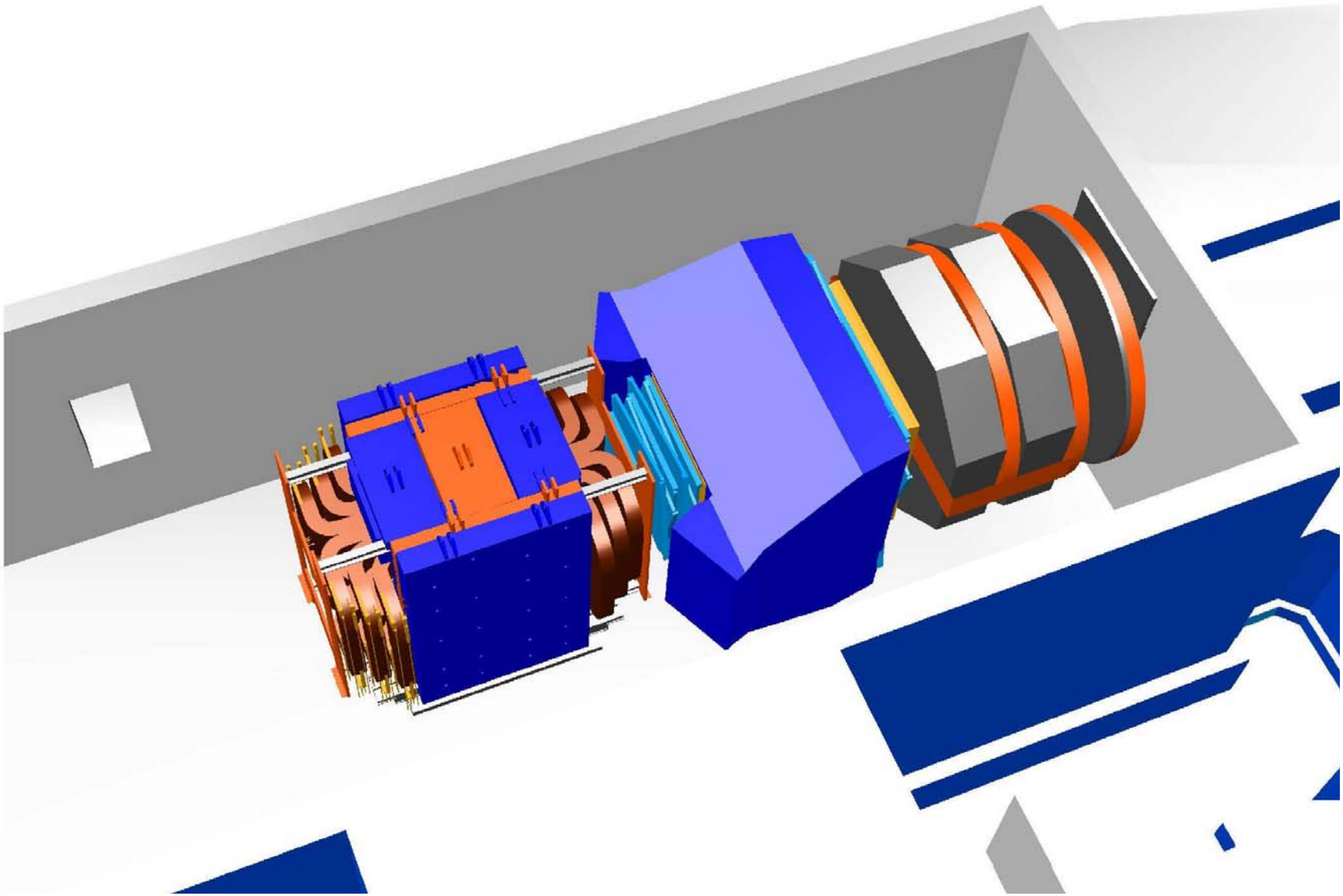
BTeV Trigger

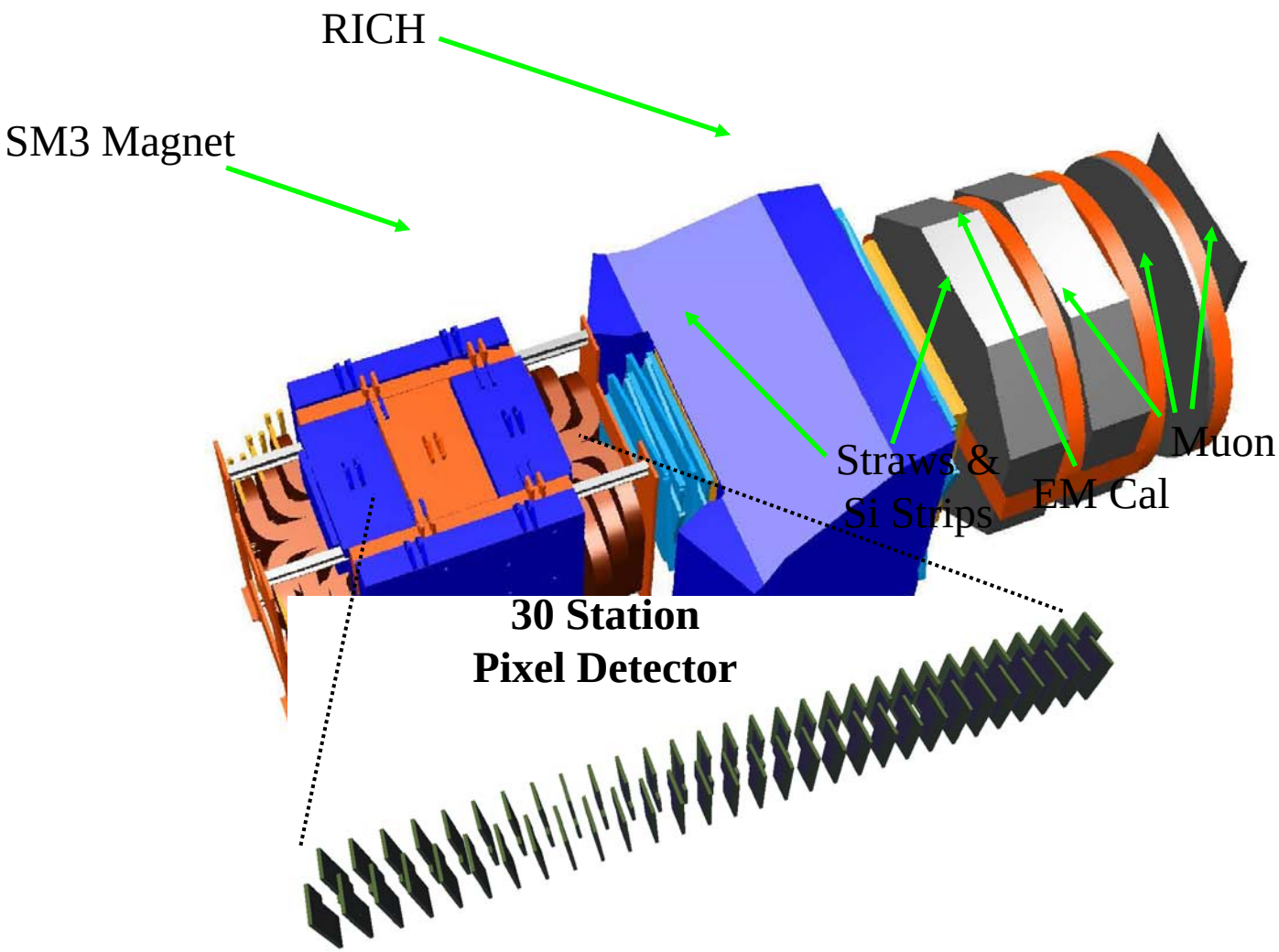
BEAUTY 2003
9th International Conference on B-Physics at Hadron Machines
Oct. 14-18, 2003, Carnegie Mellon University
Michael Wang, Fermilab
(for the BTeV collaboration)

Fermi National Accelerator Laboratory

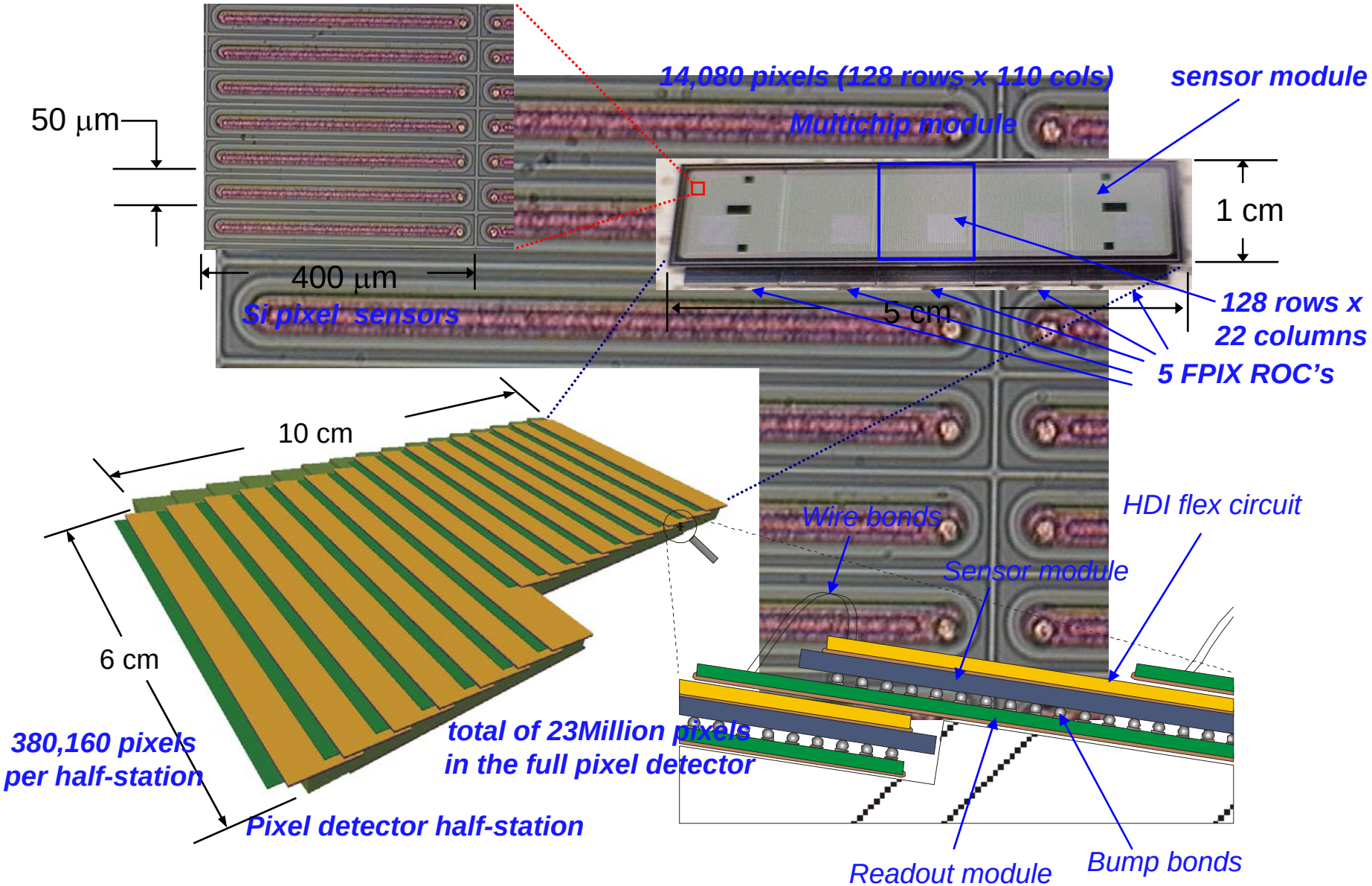


BTeV detector in the C0 collision hall

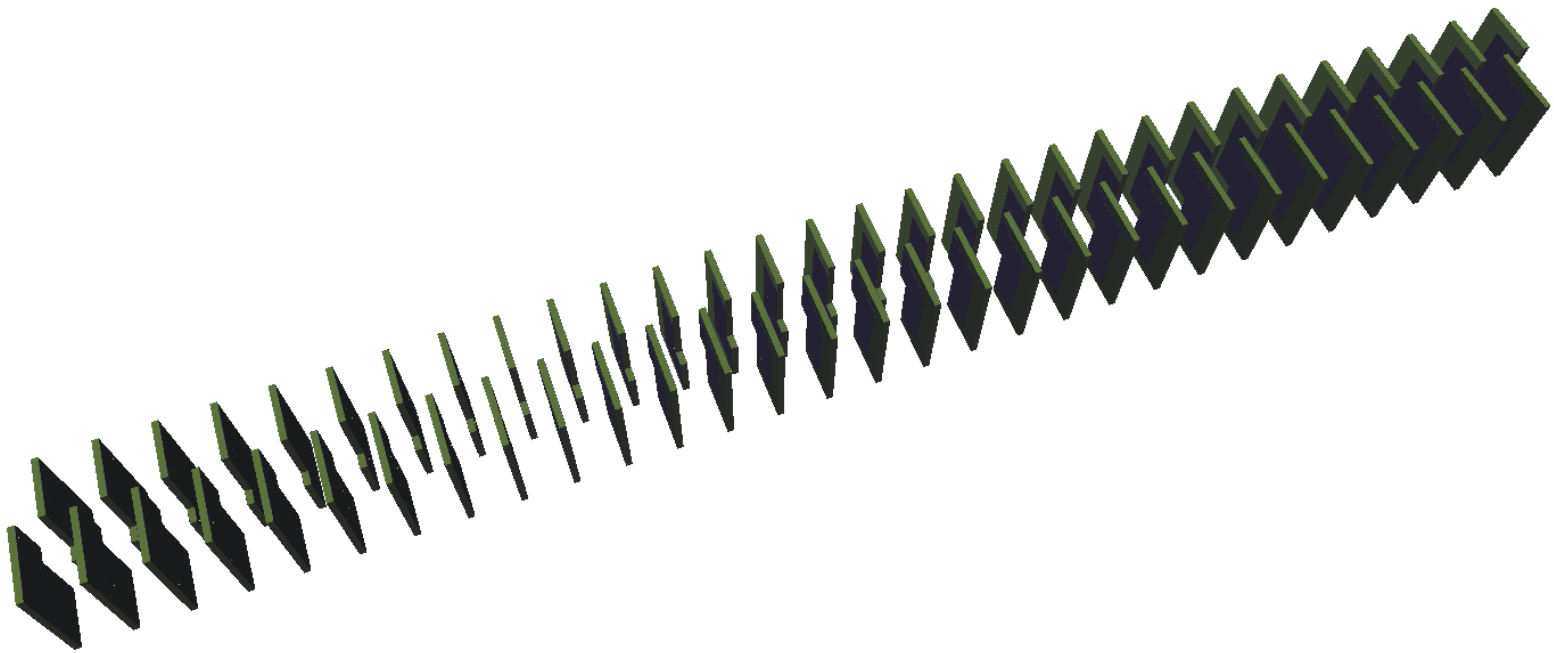



RICH
SM3 Magnet
Straws &
Si Strips
EM Cal
Muon
30 Station
Pixel Detector

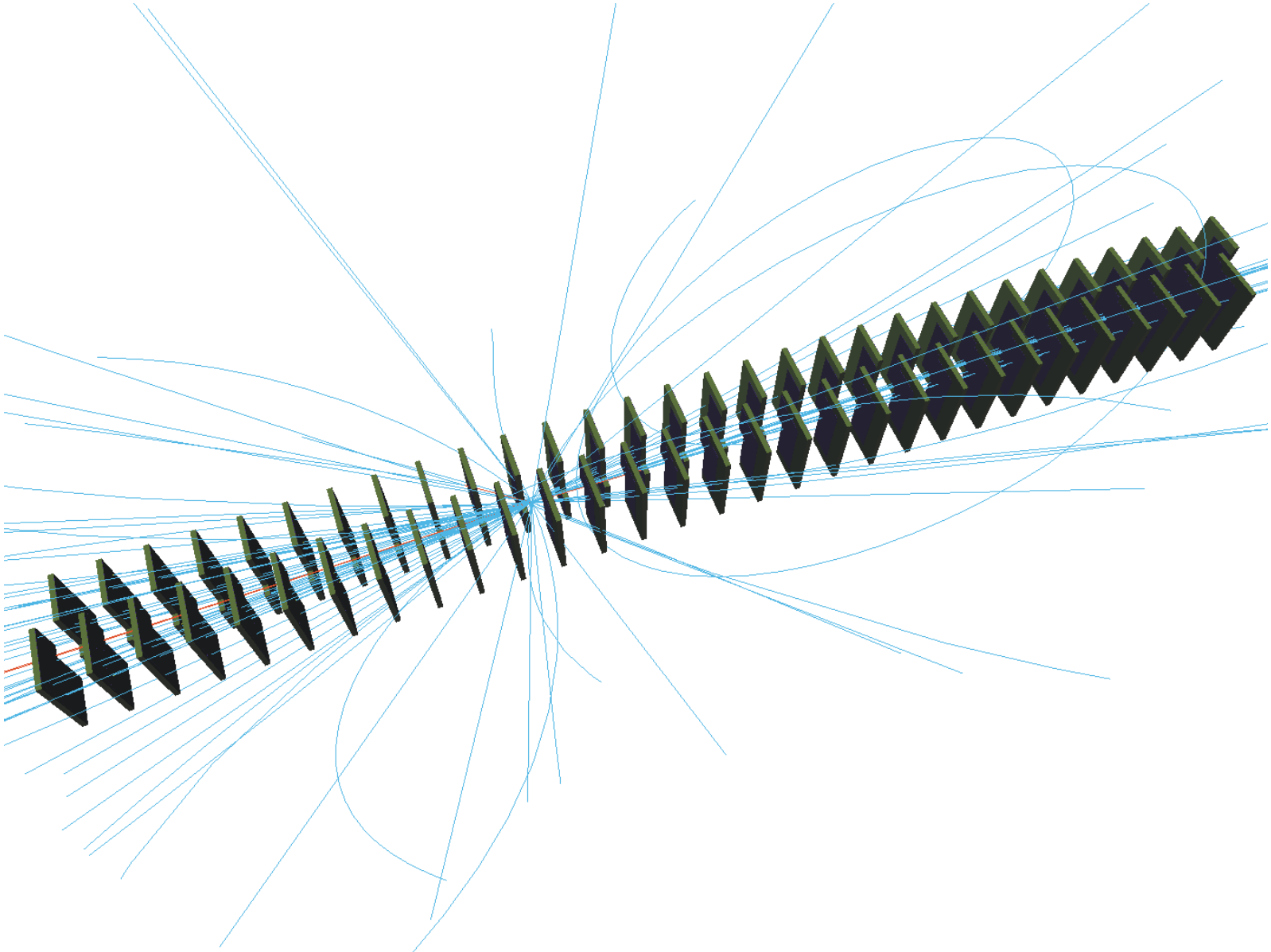
Si pixel detector



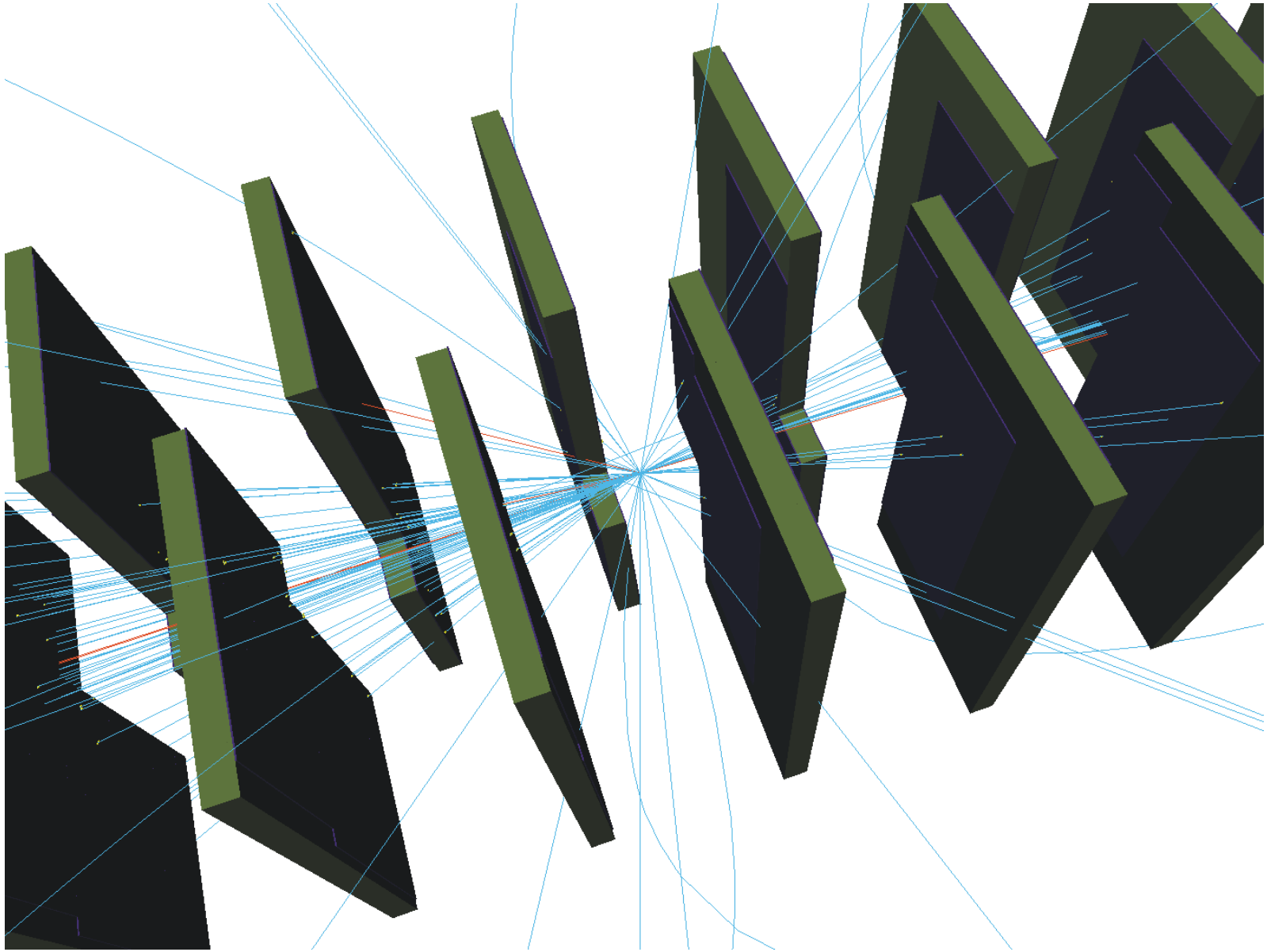
Simulated B event



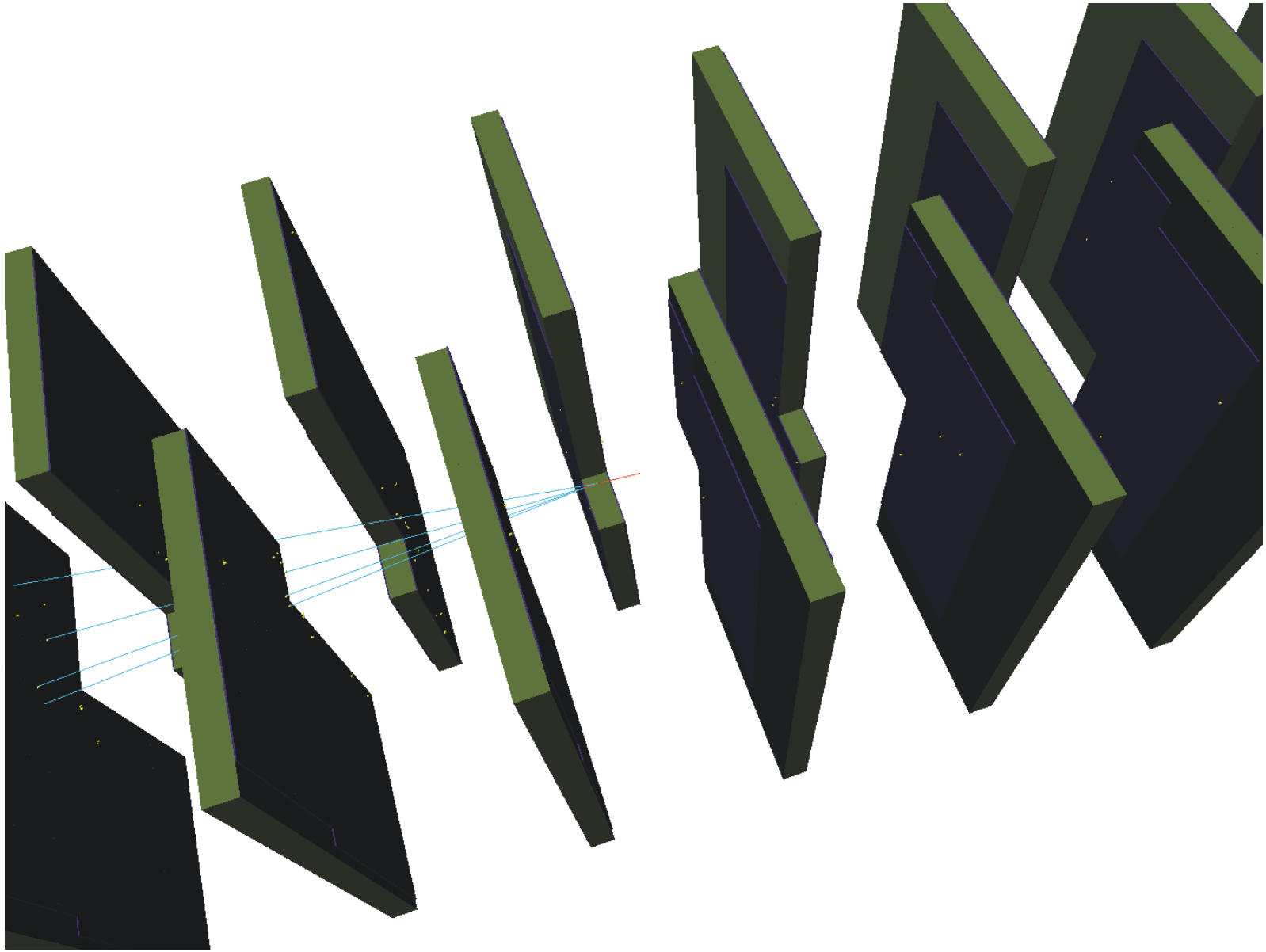
Simulated B event



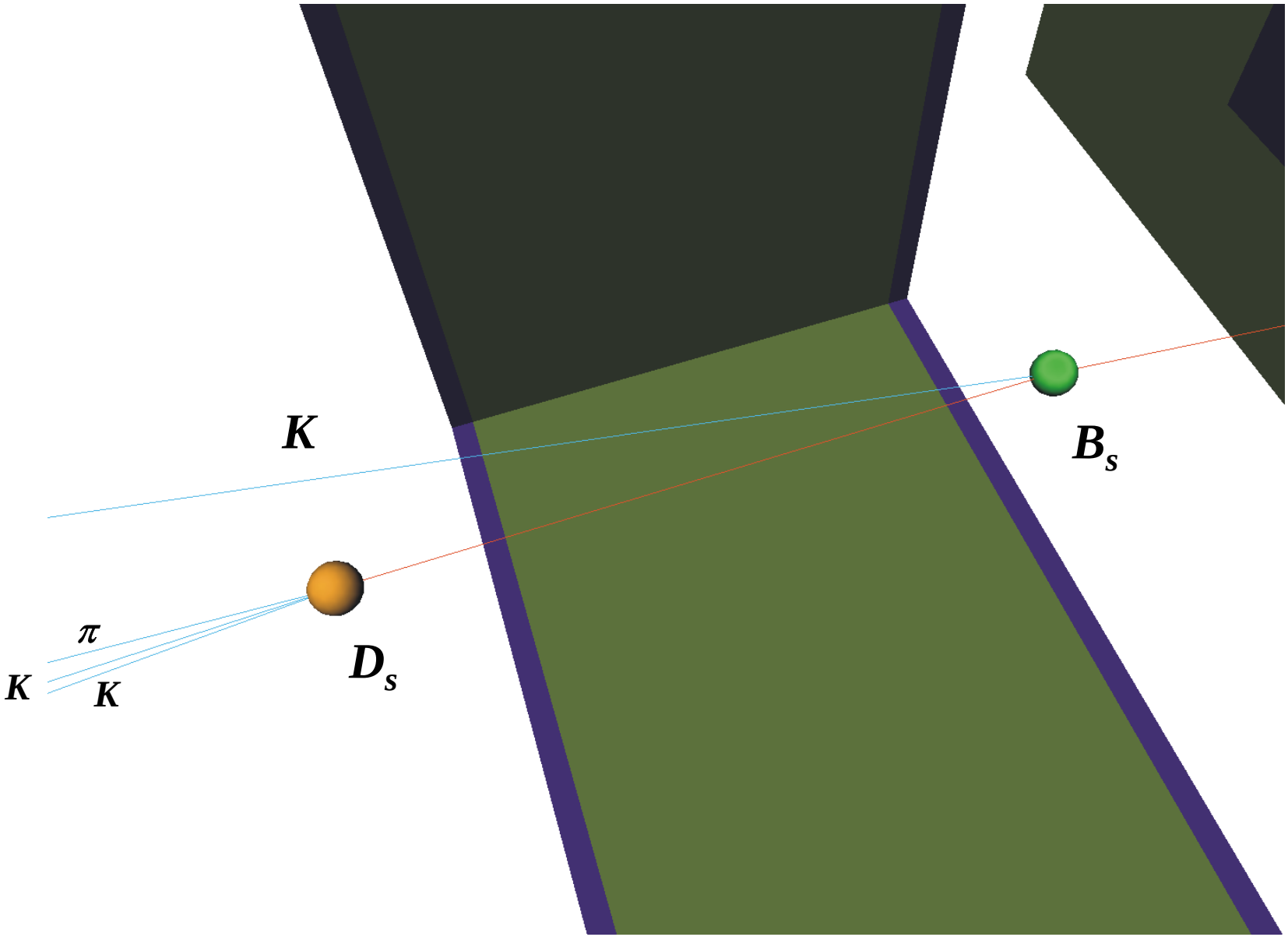
Primary interaction vertex



Primary interaction vertex

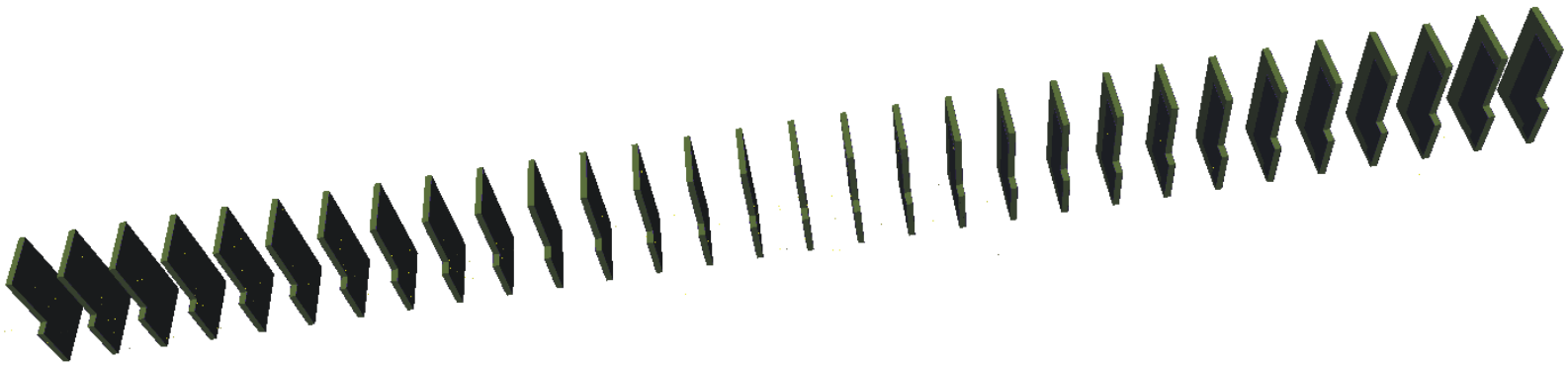


B decay vertex



Two stage trigger algorithm:

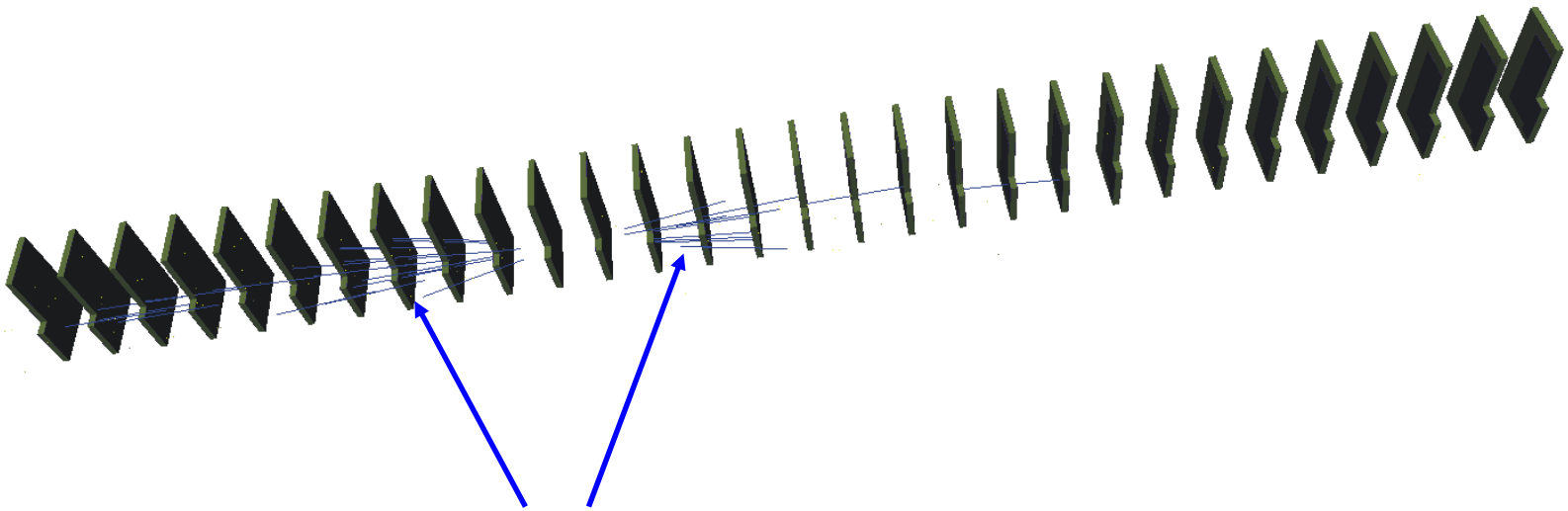
1. ***Segment finding***
2. ***Track/vertex finding***



1) <u>Segment finding stage:</u>

Use pixel hits from 3 neighboring stations to find the beginning and ending segments of tracks. These segments are referred to as triplets

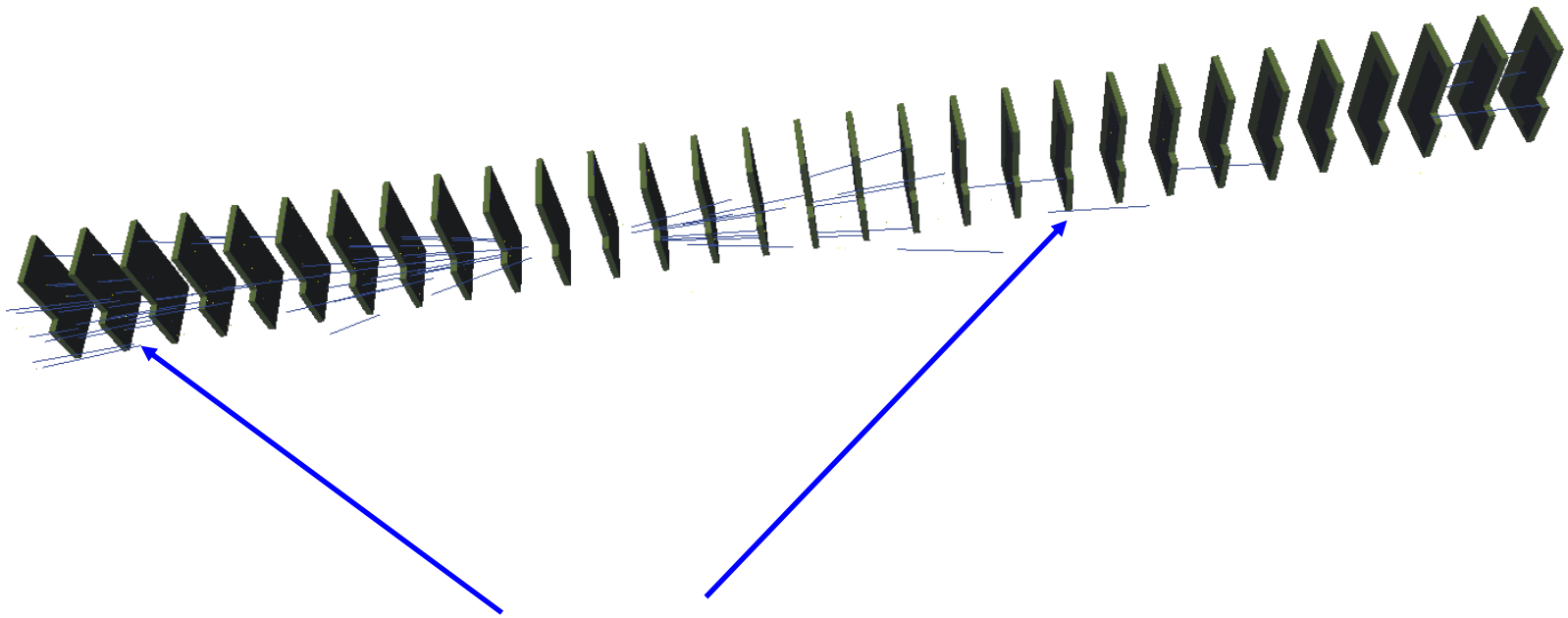
Segment finding: inner triplets



1a) <u>Segment finding stage: phase 1</u>

Start with inner triplets close to the interaction region.

An inner triplet represents the start of a track.

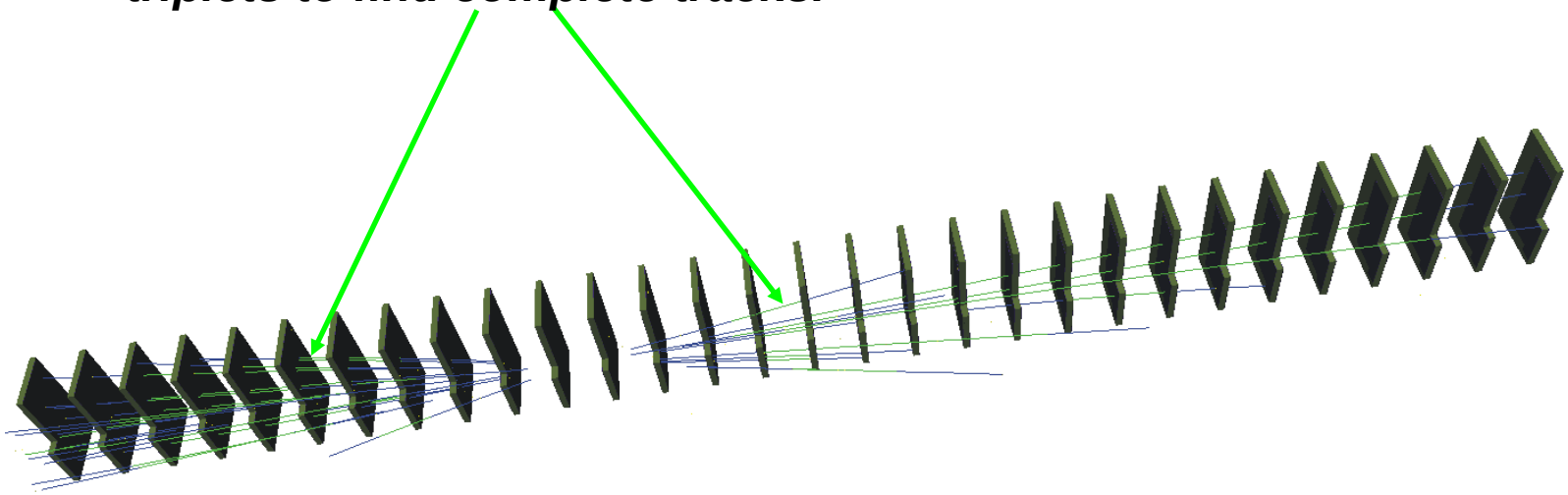


1b) <u>Segment finding stage: phase 2</u>

Next, find the outer triplets close to the boundaries of the pixel detector volume. An outer triplet represents the end of a track.

2a) <u>Track finding phase:</u>

Finally, match the inner triplets with the outer triplets to find complete tracks.



2b) <u>Vertex finding phase:</u>

- ***Use reconstructed tracks to locate interaction vertices***
- ***Search for tracks detached from interaction vertices***

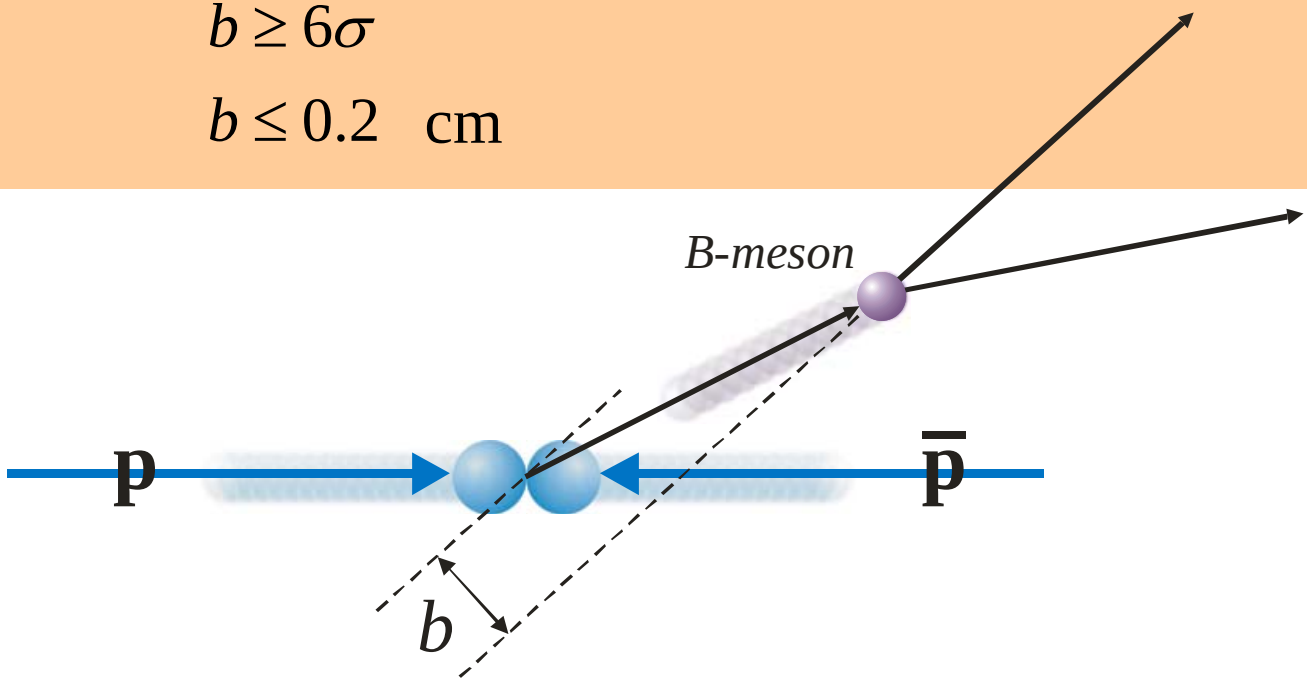
Execute Trigger

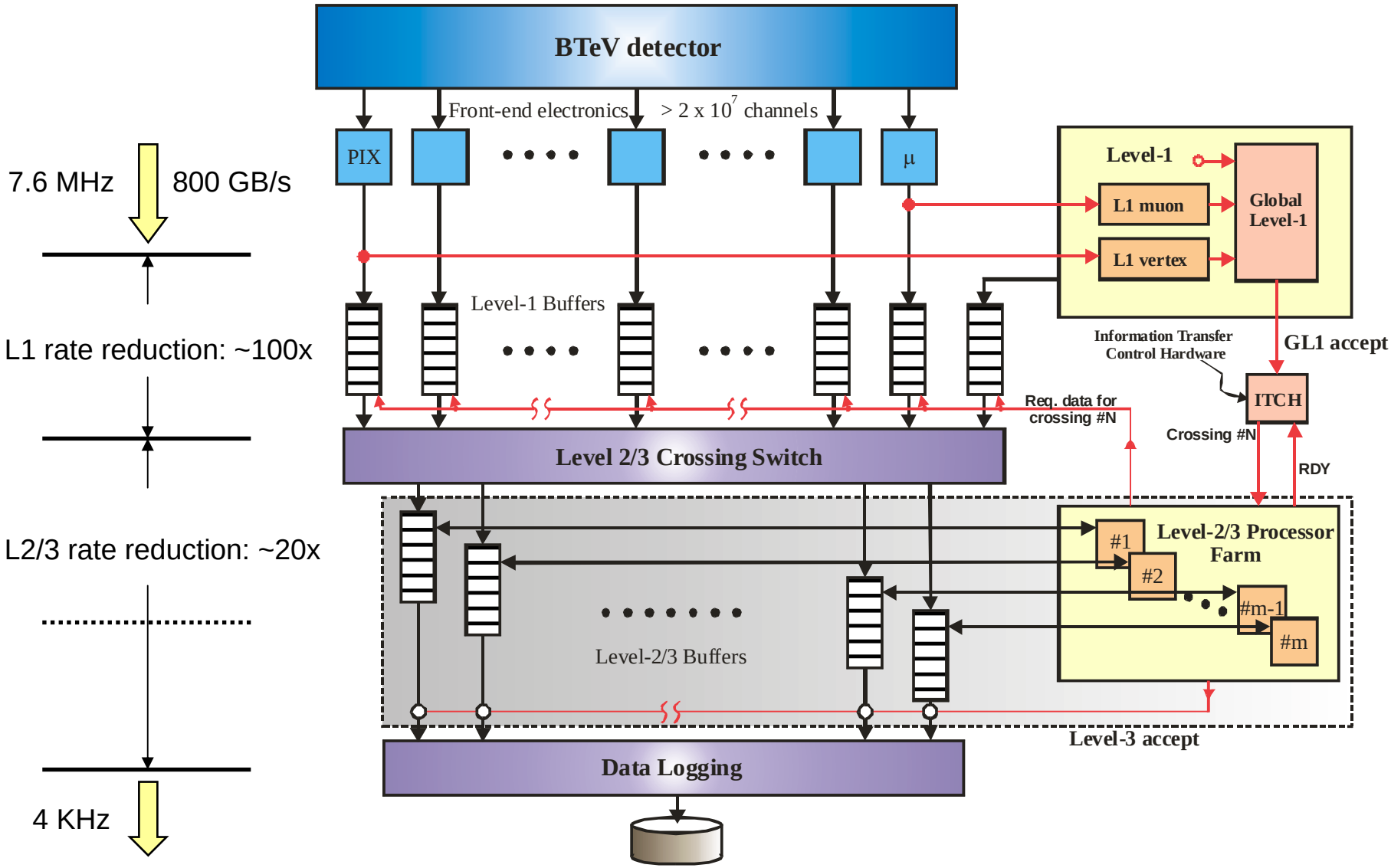
- **Generate Level-1 accept if ≥ 2 "detached" tracks going into the instrumented arm of the BTeV detector with:**

$$p_T^2 \geq 0.25 \quad (\mathrm{GeV/c})^2$$

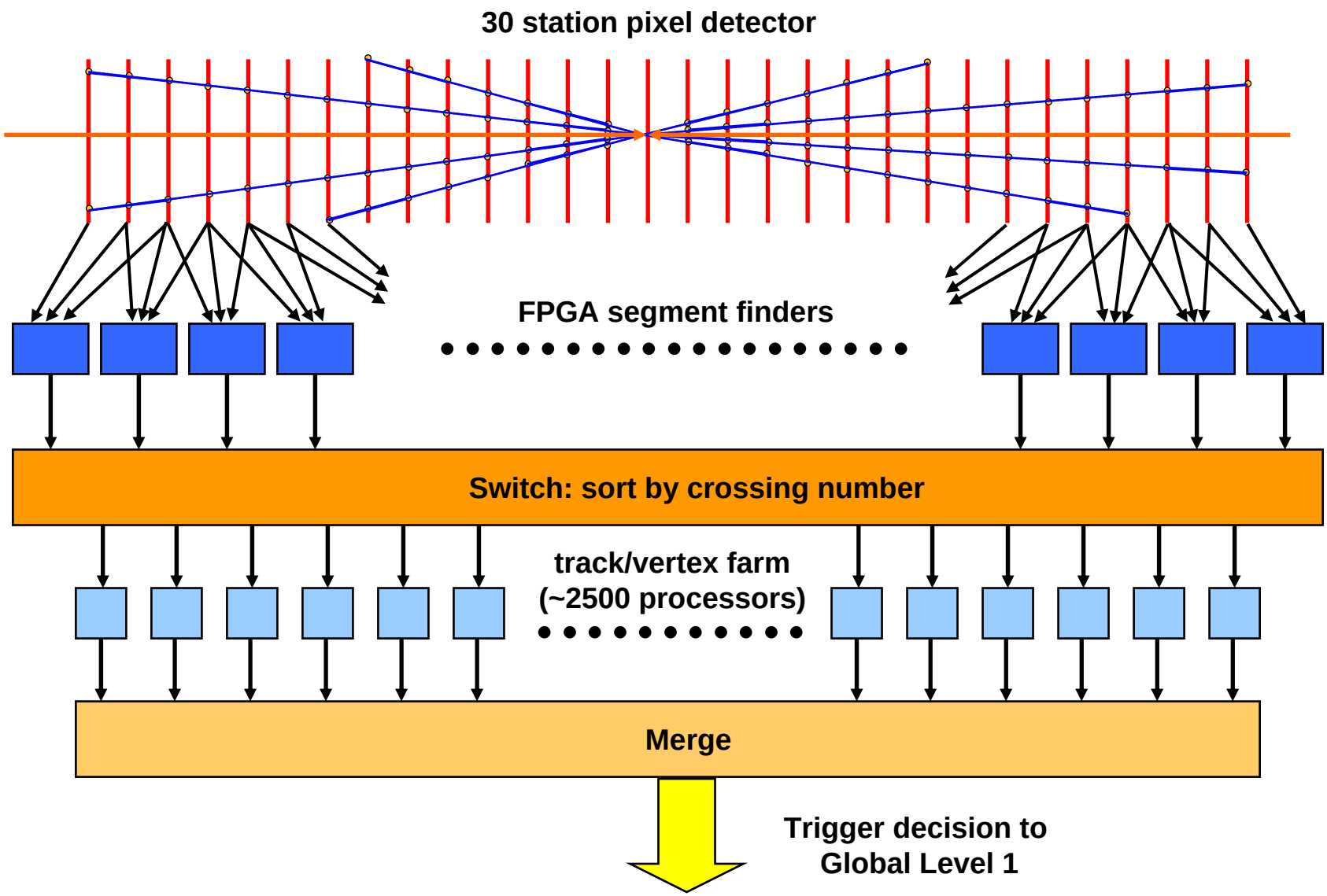
$$b \geq 6\sigma$$

$$b \leq 0.2 \quad \mathrm{cm}$$

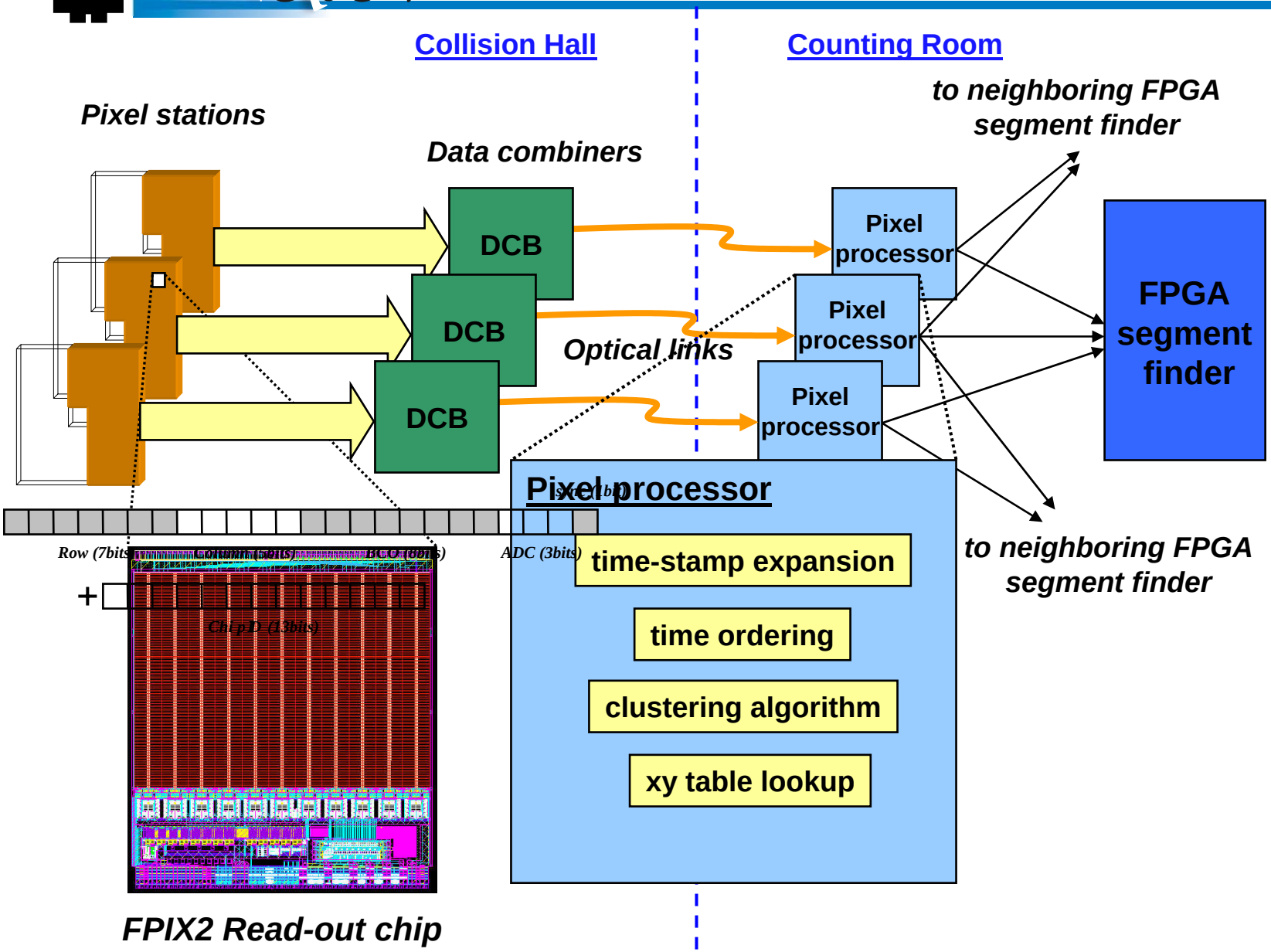



BTeV detector
Front-end electronics
> 2 x 10^7 channels
PIX
μ
7.6 MHz
800 GB/s
L1 rate reduction: ~100x
L2/3 rate reduction: ~20x
4 KHz
Level-1
L1 muon
L1 vertex
Global Level-1
Level-1 Buffers
Information Transfer Control Hardware
GL1 accept
ITCH
Req. data for crossing #N
Crossing #N
RDY
Level 2/3 Crossing Switch
Level-2/3 Processor Farm
#1
#2
#m-1
#m
Level-2/3 Buffers
Level-3 accept
Data Logging

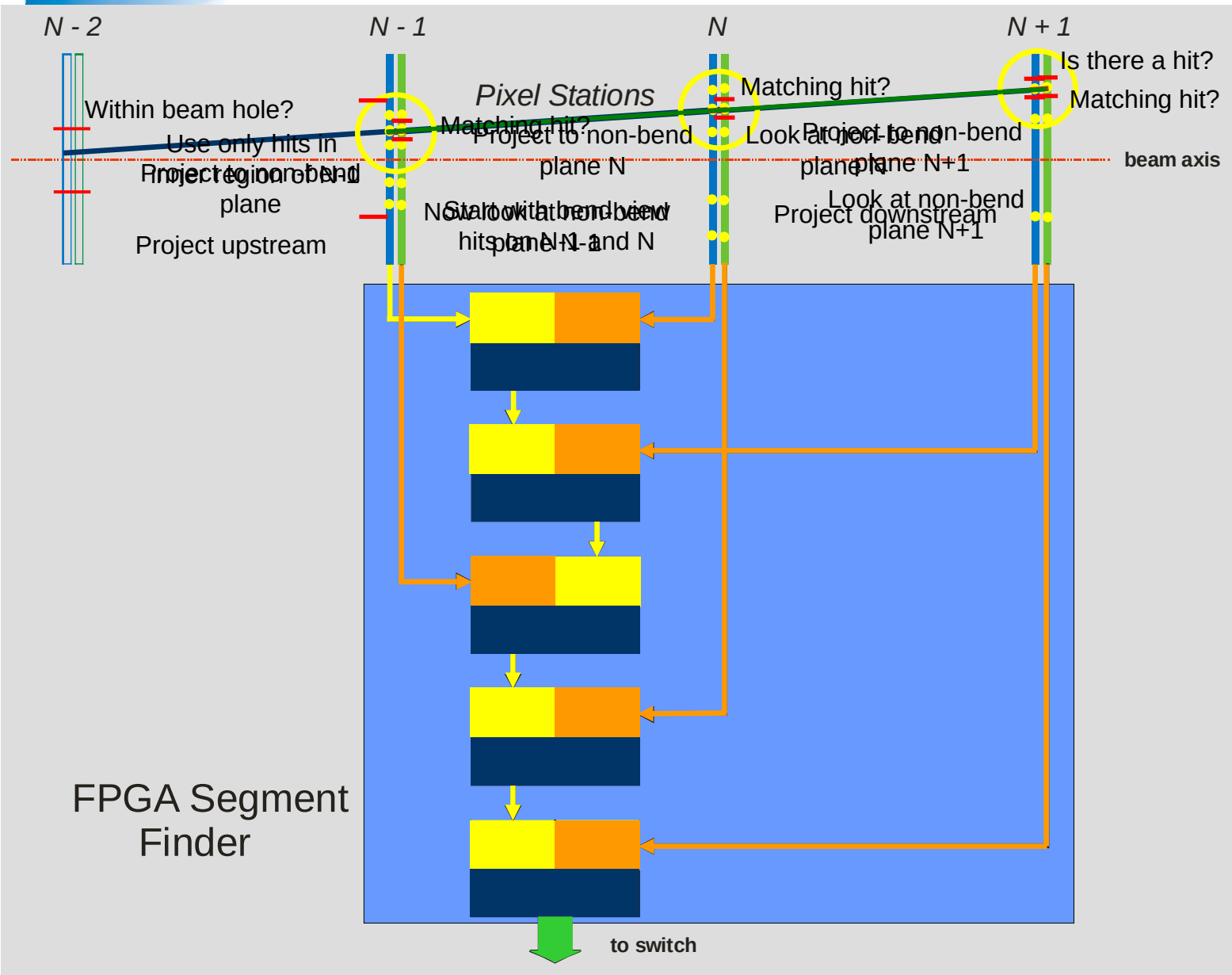
Level 1 vertex trigger architecture



Pixel data readout

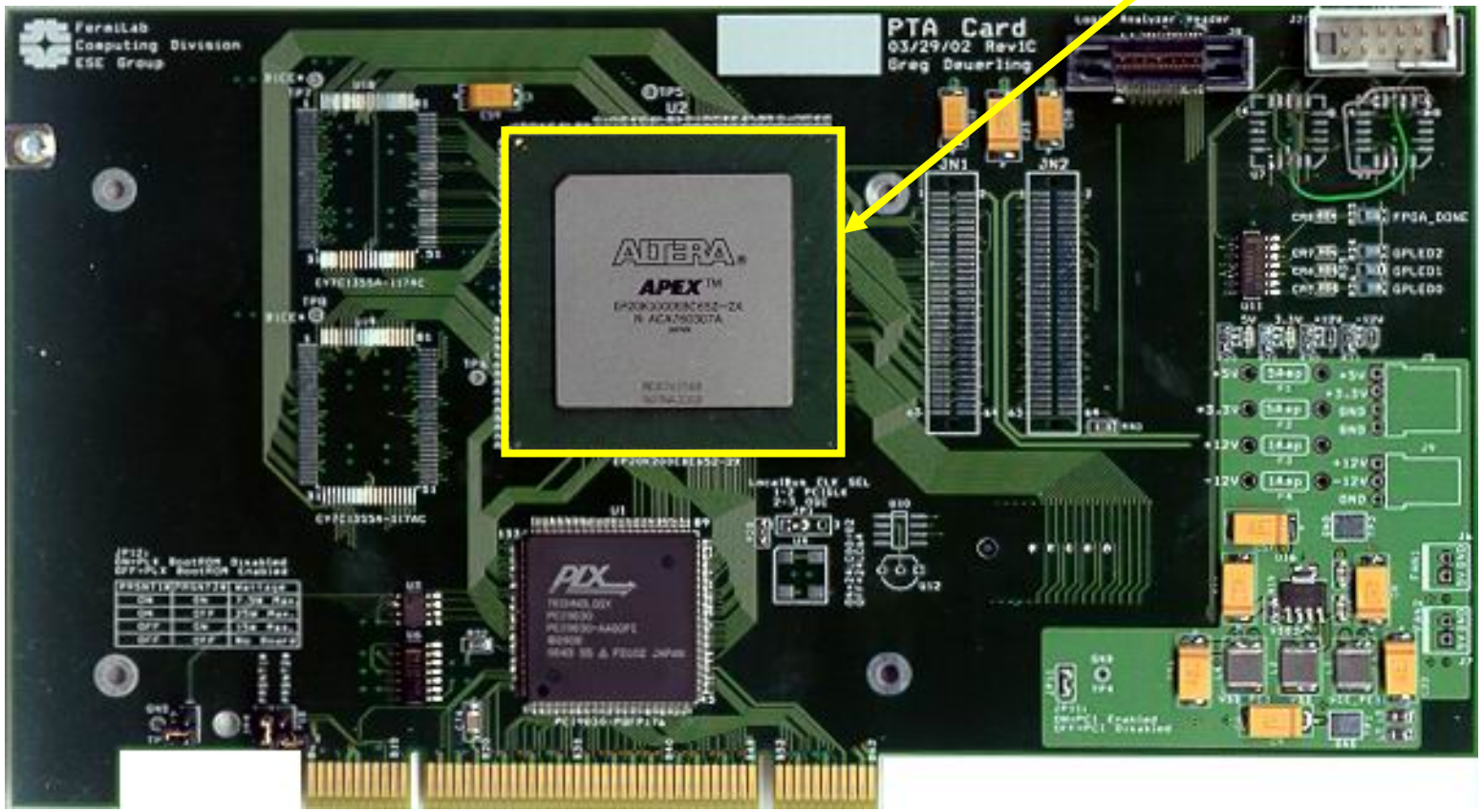


L1 segment finder hardware

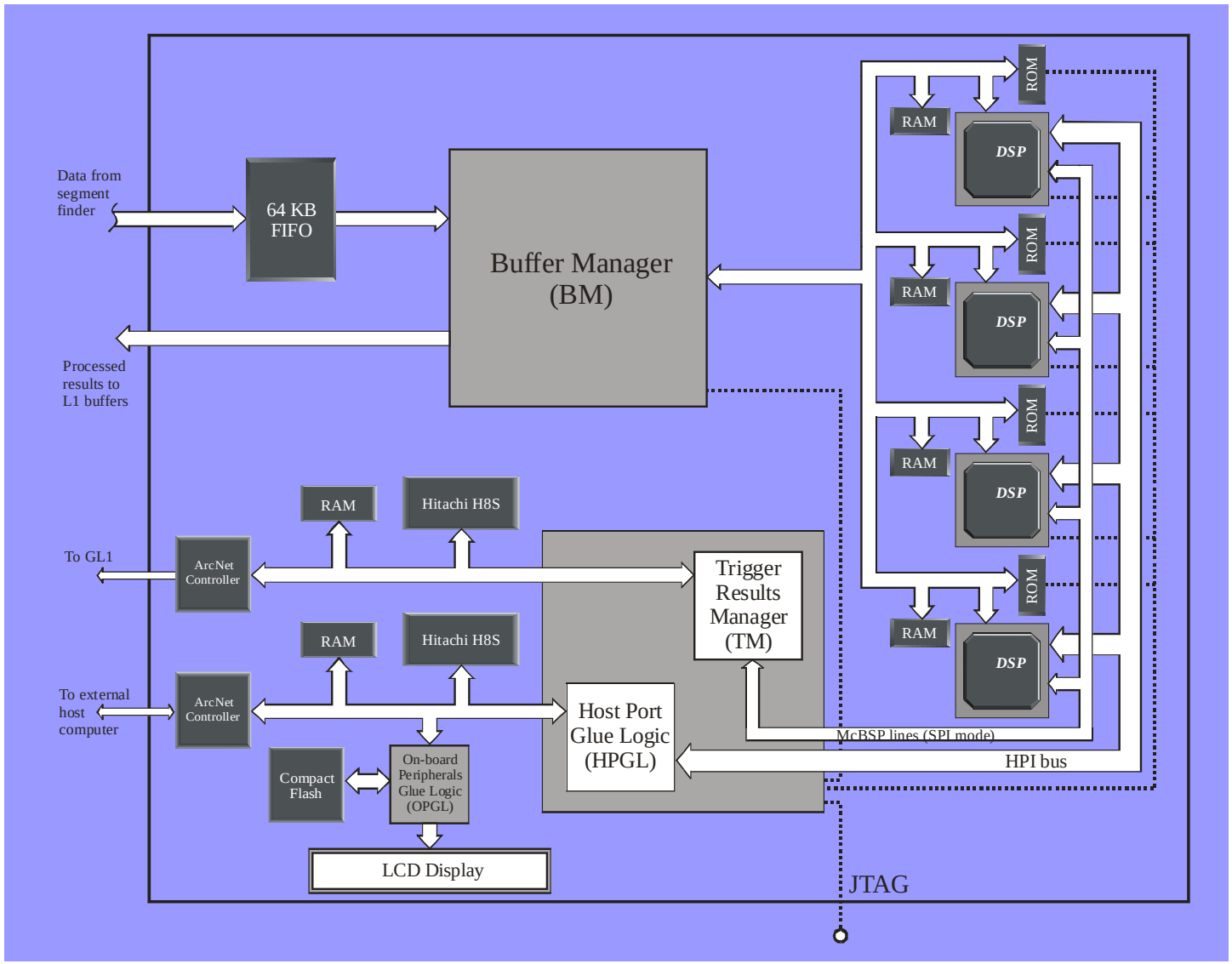


L1 segment finder on PTA card

Uses Altera APEX EPC20K1000 instead of EP20K200 on regular PTA

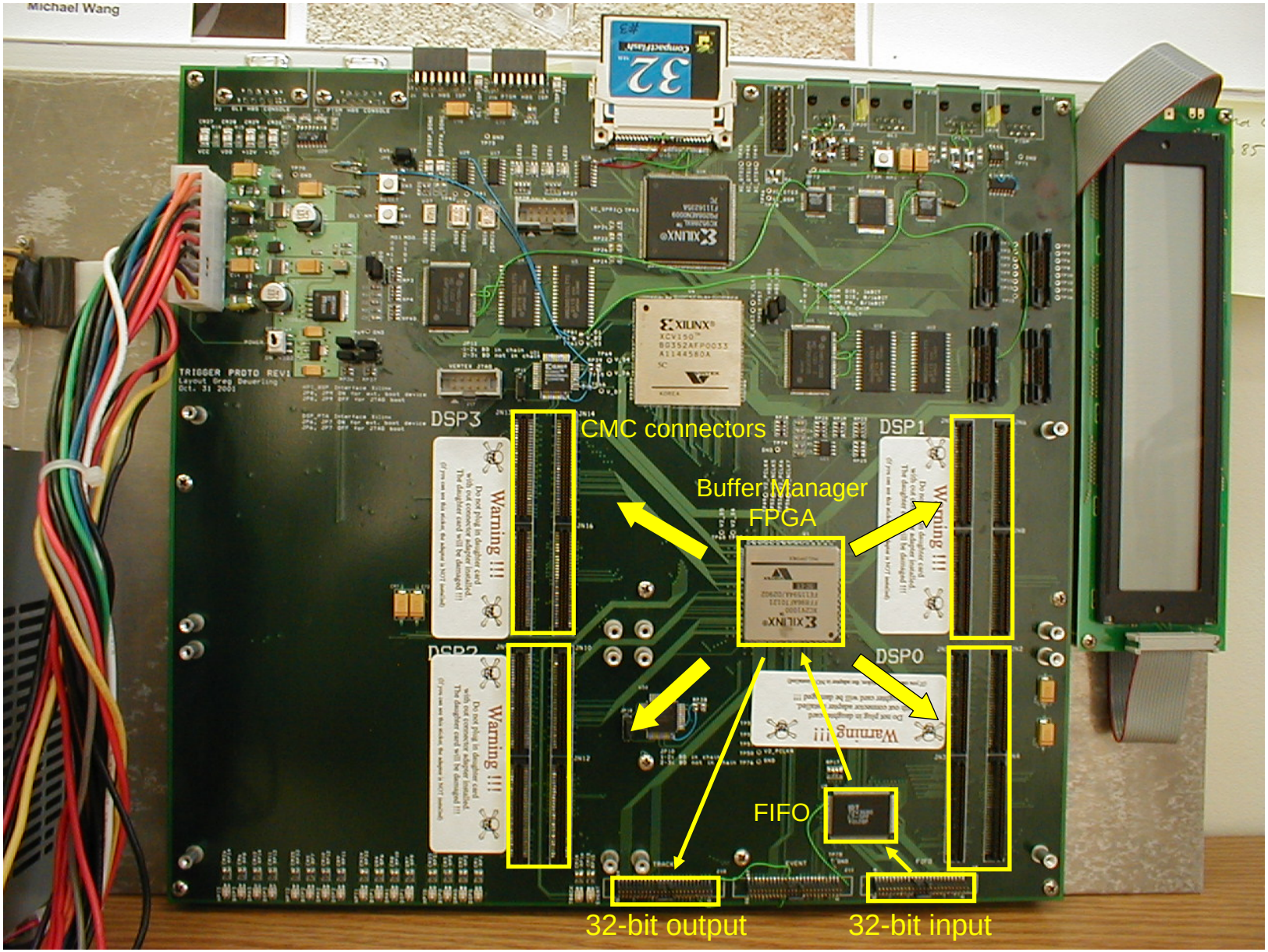


Modified version of PCI Test Adapter card developed at Fermilab for testing hardware implementation of 3-station segment finder (a.k.a. “Super PTA”)

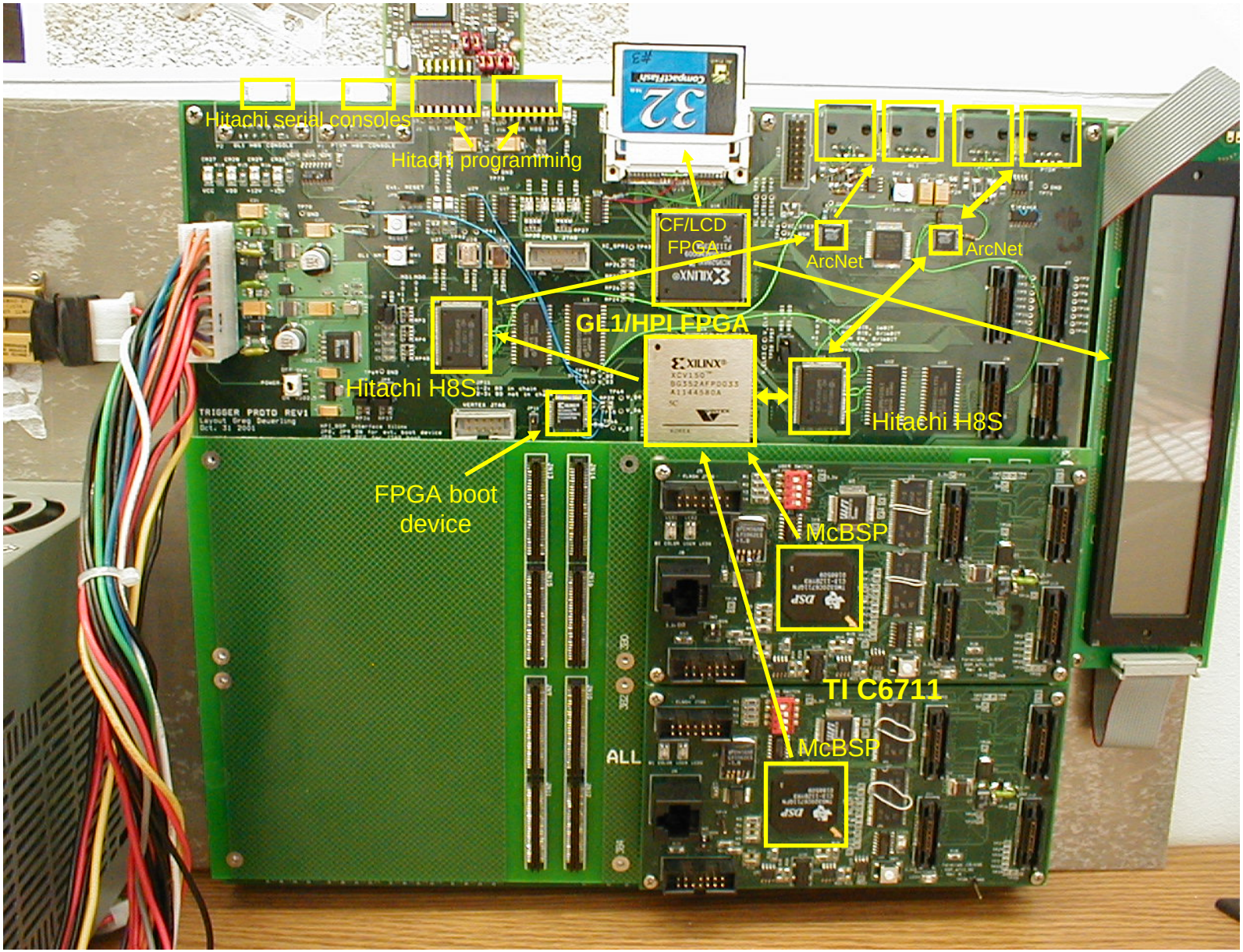


Block diagram of pre-prototype L1 track/vertex farm hardware

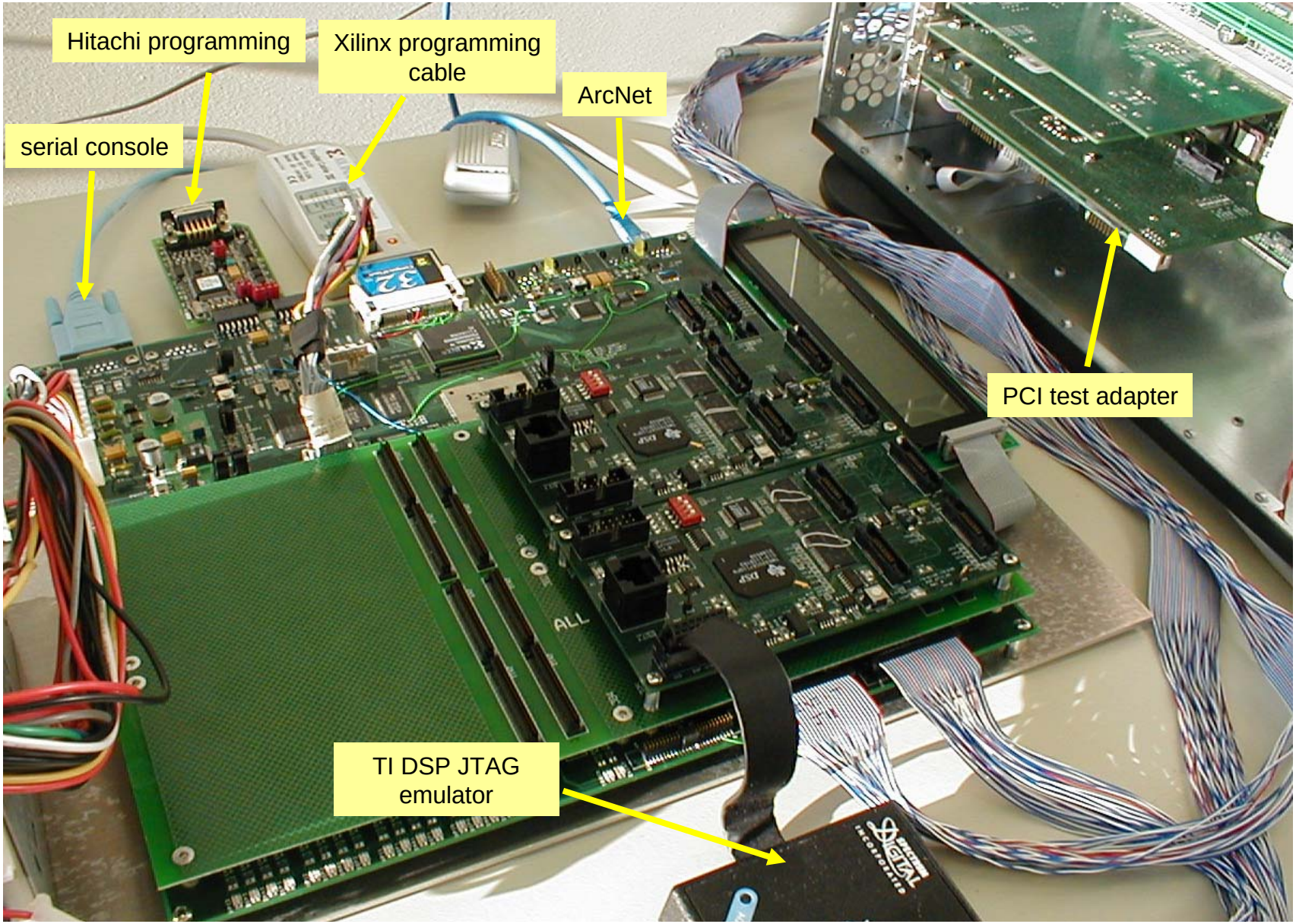
L1 trigger pre-prototype board



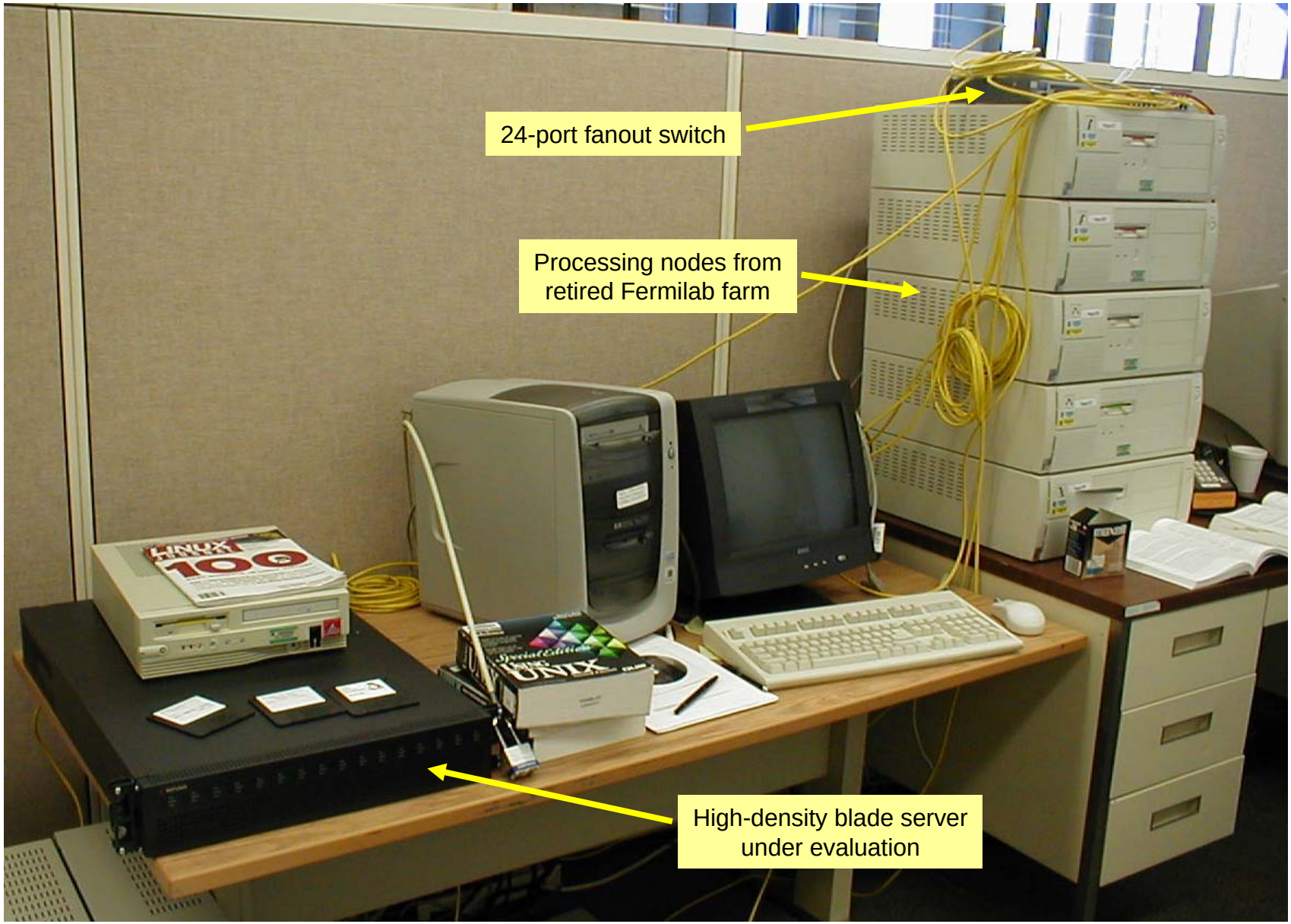
L1 pre-prototype with DSP mezzanine cards



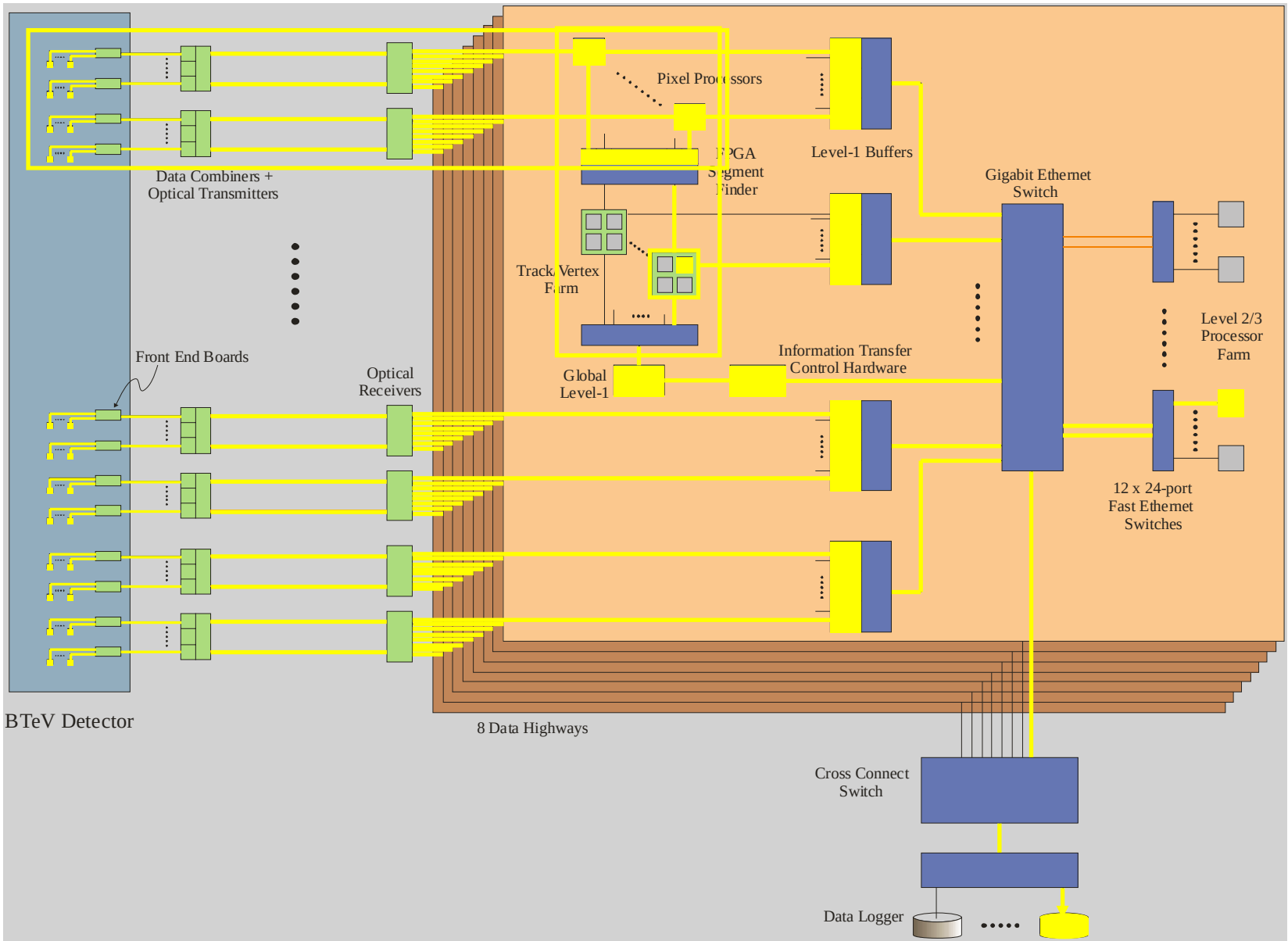
L1 trigger pre-prototype test stand



Level 2/3 trigger R&D

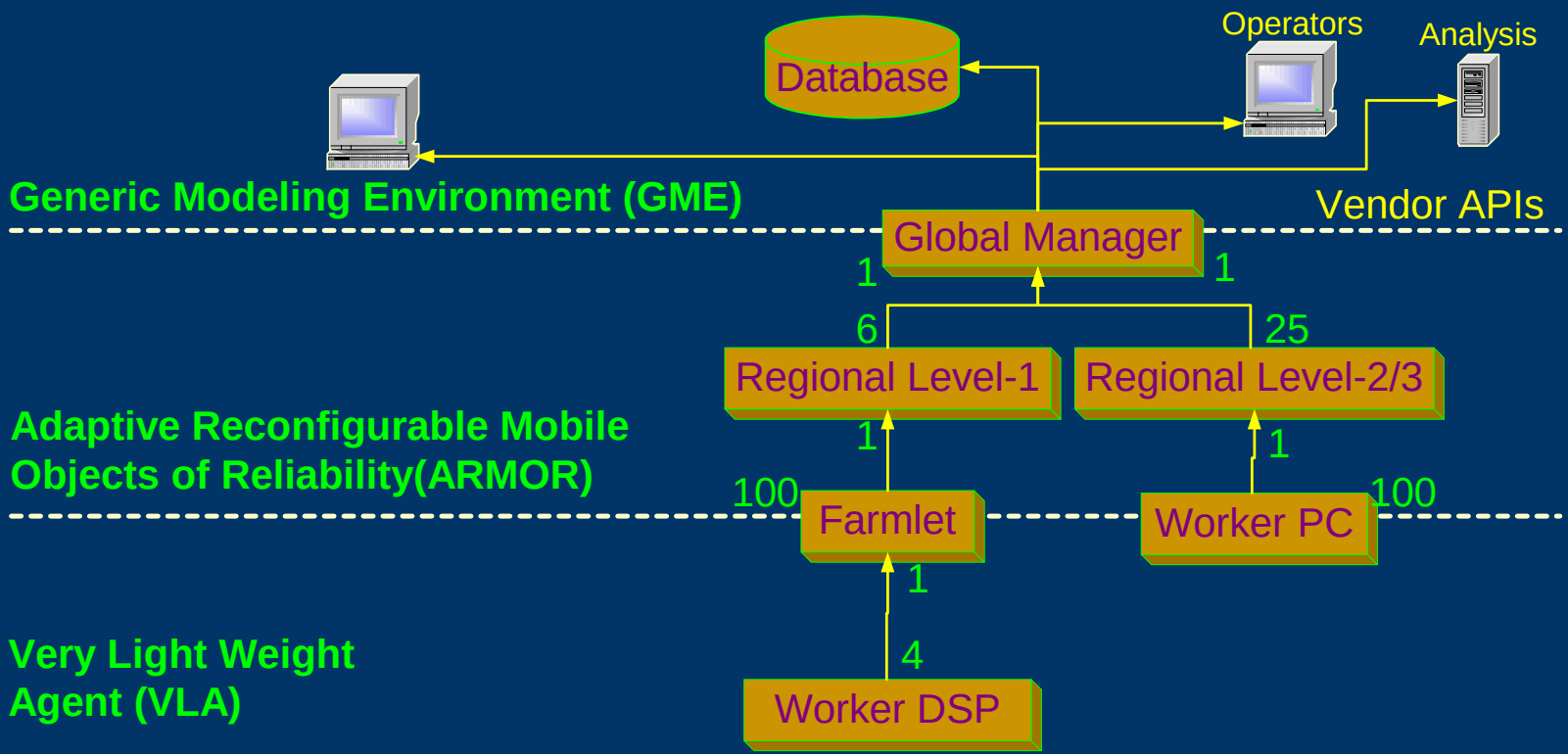


BTeV trigger architecture



Real Time Embedded Systems (RTES)

- RTES: NSF ITR (Information Technology Research) funded project
- Collaboration of computer scientists, physicists & engineers from: Univ. of Illinois, Pittsburgh, Syracuse, Vanderbilt & Fermilab
- Working to address problem of reliability in large-scale clusters with real time constraints
- BTeV trigger provides concrete problem for RTES on which to conduct their research and apply their solutions



End

Backup slides

Process	Efficiency
Minimum bias	1%
$B_s \rightarrow D^+_s K^-$	80%
$B^0 \rightarrow J/\psi K_s$	65%
$B^- \rightarrow K_s \pi^-$	45%
$B^- \rightarrow \phi K_s$	74%
$B^0 \rightarrow$ 2-body modes $(\pi^+\pi^-, K^+\pi^-, K^+K^-)$	80%

L1 vertex trigger efficiencies

Process	Efficiency
Light quark	7%
$B_s \rightarrow D^+_s K^-$	85%
$B^0 \rightarrow J/\psi K_s$	78%
$B^- \rightarrow K_s \pi^-$	72%
$B^- \rightarrow \pi^+ \pi^-$	87%

L2/L1 trigger efficiencies